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OPERATION AND MAINTENANCE INSTRUCTIONS FOR WJ-1204-1 SYNTHESIZED SIGNAL GENERATOR

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WATKINS-JOHNSON

3333 Hillview Avenue
Stanford Industrial Park
Palo Alto, California 94304

SSE–975

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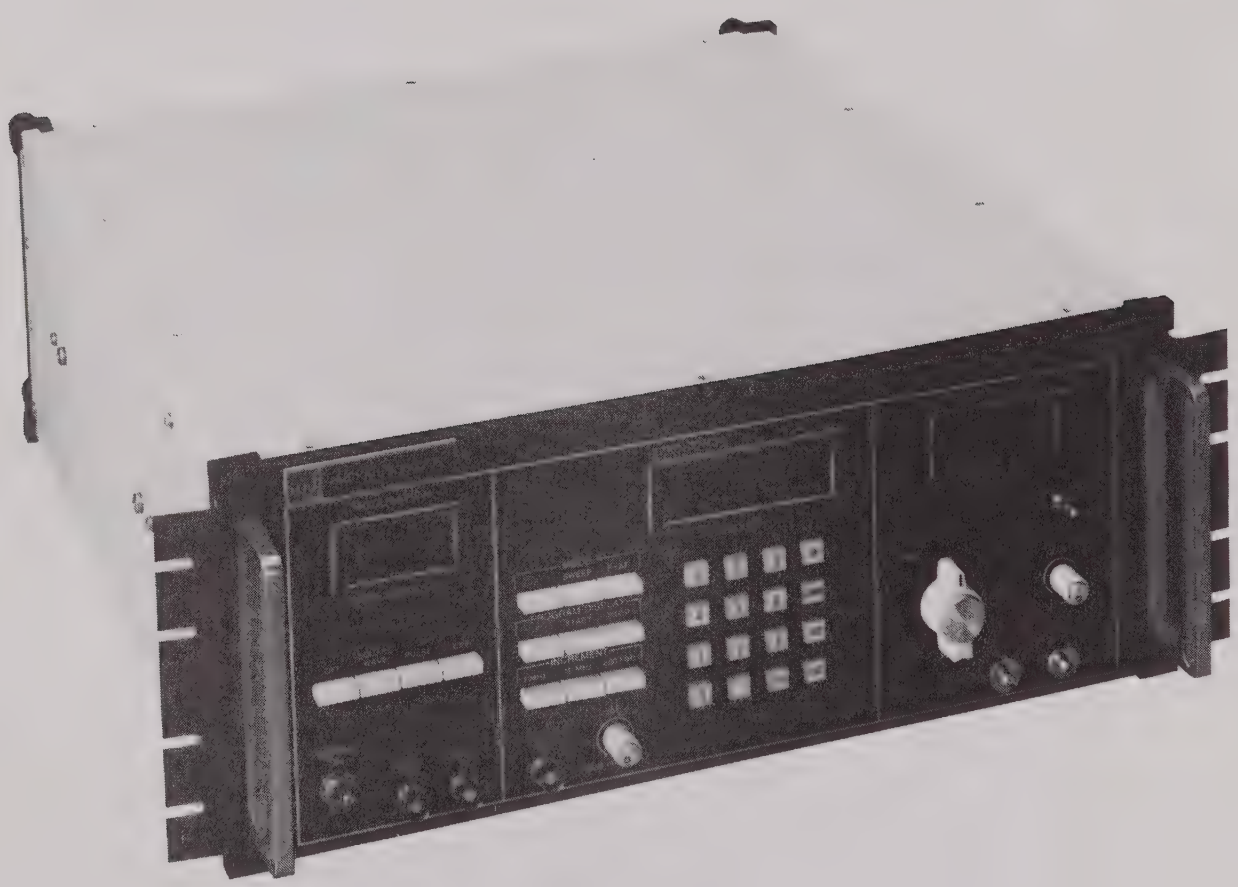

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Figure 1-1. WJ-1204-1 Synthesized Signal Generator

CHAPTER 1

GENERAL INFORMATION AND SAFETY PRECAUTIONS

1-1. SAFETY PRECAUTIONS. The following are general safety precautions that are not related to any specific procedures and therefore, do not appear elsewhere in this publication. These are recommended precautions that personnel must understand and apply during many phases of operation and maintenance. Operating personnel must at all times observe all safety regulations. Do not replace components inside equipment with the power cord plugged in. Under certain conditions, dangerous potentials may exist when the power control is in the OFF position, due to charges retained by capacitors. Always remove power and discharge or ground a circuit before touching it.

WARNING

115/230 volts ac is used in this instrument. Some of the maintenance and servicing operations described herein are performed with power supplied to the instrument while protective covers are removed. Exercise extreme care when performing these operations. Line voltage is always present on terminals including the power input connector, fuse holder, power switch, etc. In addition, when the instrument is on, energy available at many points may result in personal injury or death when contacted.

WARNING

This instrument is supplied with a three-wire power cable. The center third wire is intended to connect the instrument chassis to earth ground when used with a properly wired three-conductor outlet. Refer to Chapter 8 for details of power connection. Improperly grounded equipment configurations may result in hazardous potentials between the chassis of two or more instruments or earth ground.

CAUTION

Input circuits at the EXT RF IN connector can be destroyed with input levels exceeding +15 dBm (31.6 mW).

NOTE

Personnel working with or near high voltages should be familiar with modern methods of RESUSCITATION. Such information may be obtained from the Bureau of Medicine and Surgery.

1-2. INTRODUCTION. The purpose of this manual is to provide information regarding the operation, installation, and maintenance of the WJ-1204-1 Synthesized Signal Generator. This chapter provides general information for the WJ-1204-1 Synthesized Signal Generator and includes a statement of the purpose of the unit, a description of the unit, and a list of the equipment and documents supplied.

WARRANTY

This instrument is warranted against defects in materials and workmanship for a period of one year from the date of delivery. The manufacturer will replace or repair the instruments in accordance with the terms outlined in the Product Warranty statement shipped with each unit.

1-3. PURPOSE OF UNIT. The purpose of the WJ-1204-1 Synthesized Signal Generator is to provide broadband frequency coverage from a single unit, provide internal pulse and square wave modulation, and measure internal and external RF power. It is designed primarily for making maintenance and performance tests on electronic countermeasure (ECM) and receiving equipment. The WJ-1204-1 is for use by maintenance personnel for testing installed radar, receiving, and electronic warfare (EW) systems. It has the capability of generating sweep frequencies which is very useful as a pseudo noise source. Typical applications for the WJ-1204-1 are sensitivity measurements, return loss (VSWR), frequency measurements, power measurements, and receiver alignment. Because of its compact size and weight, this instrument is excellent for testing ECM and receiving systems in closely confined areas.

1-4. EQUIPMENT DESCRIPTION. The WJ-1204-1 (figure 1-1) is a combination of a frequency synthesizer and a signal generator. It provides extremely accurate (0.005% for 180 days) frequency coverage in the 0.1 to 26 GHz range, and has modulation and output level control capabilities. The stable, spectrally pure output signal is obtained by phase locking a voltage controlled oscillator (VCO) to a 5 MHz reference signal. An internal yttrium iron garnet (YIG)-tuned mulitplier receives signals from the VCO, and in conjunction with a frequency doubler, provides the 2-26 GHz frequency coverage. The RF output power is internally leveled and calibrated from 0 dBm to -20 dBm. All control settings are located on the front panel along with two light-emitting diode (LED) displays: FREQUENCY and RF POWER (dBm).

1-5. REFERENCE DATA. Reference data which includes the electrical and environmental capabilities and limitations of the WJ-1204-1 are listed in table 1-1.

Table 1-1. Reference Data

Characteristic	Specification
Manufacturer	Watkins-Johnson Company
Type	Synthesized Signal Generator
Model	WJ-1204-1

Table 1-1. Reference Data -Continued

Characteristic	Specification
Frequency Range	0.1 to 26 GHz
Frequency Stability	5×10^{-6}/year aging rate, and $\pm 1 \times 10^{-6}$ over 0 °C to 50 °C temperature range or as determined by external 5 MHz reference oscillator.
Frequency Display	Five-digit LED display with floating decimal.
Frequency Resolution	10 kHz from 100 to < 250 MHz 100 kHz from 250 MHz to < 2 GHz 1 MHz from 2 to 26 GHz
Frequency Accuracy	0.005% for a calibration period of 180 days.
Reference Standard	5 MHz internal/external.
Modes of Operation	Discrete, Sweep, $F \pm \Delta F$
Remote Programming (Option AB)	GPIB Compatible (IEEE STD-488/1978)
Modulation	a. 1 kHz square wave b. 0.1 to 10 μs pulse width with 0.1 μs increments, 1 kHz PRF c. External d. External Sync Output
Output Power Leveled Accuracy*	 0 dBm 0.1 to 26 GHz ± 1 dB
Calibrated Attenuator	0 to -90 dB, in 10 dB steps
Power Adjustment	Greater than 10 dB, continuous adjustment, 0.1 dB resolution via front panel adjust potentiometer and power measurement readout.
Power Measurement Range (Internal/External)	 -30 dBm to +10 dBm
Spectral Purity	Harmonic, subharmonics and nonharmonically related spurious less than -40 dBc.
Sweep	Narrowband continuous. Narrow to wideband stepped.

*The accuracy of ±1 dB is only applicable when the ATTENUATION (dB) control is in the 0 dB position. In positions 10 dB through 90 dB, the accuracy of the displayed power must account for the accuracy of the Step Attenuator. In the frequency range of 0.1 to 18 GHz, the accuracy of the Step Attenuator is ±1.0 dB. The total accuracy thus becomes ±2.0 dB. In the range of 18 to 26 GHz, the accuracy of the Step Attenuator is ±1.5 dB for the total accuracy of ±2.5 dB as displayed on the LED readout.

Table 1-1. Reference Data -Continued

Characteristic	Specification
Sweep Increments	1, 10, and 100 MHz
Power Requirements	115/230 ±10% Vac, 47-420 Hz, 250 VA
Environmental Temperature	0 °C to 50 °C operating; -40 °C to +75 °C storage.
Relative Humidity	95% noncondensing
Altitude	To 40,000 ft (12,000 m)

1-6. EQUIPMENT, ACCESSORIES, AND DOCUMENTATION SUPPLIED. Table 1-2 lists the equipment, accessories, and documents supplied with the WJ-1204-1.

1-7. EQUIPMENT AND PUBLICATIONS REQUIRED BUT NOT SUPPLIED. Table 1-3 lists the equipment that is required, but not supplied, to maintain the WJ-1204-1.

1-8. FIELD CHANGES AND FACTORY CHANGES. Tables 1-4 and 1-5 provide for entries of field and factory changes according to change number, nomenclature of part affected, and description of change and its purpose.

Table 1-2. Equipment, Accessories, and Documentation Supplied

Quantity	Nomenclature	Unit number	Overall dimensions	Weight and volume
1	Synthesized Signal Generator	Model WJ-1204-1	Uncrated Height 6.5 in. Depth 19.6 in. Width 17.0 in. Crated Height 13.0 in. Depth 29.0 in. Width 24.0 in.	Uncrated Weight 35 lb Volume 1.25 ft^3 Crated Weight 42 lb Volume 5.2 ft^3
2	Technical Manual	SSE-975	N/A	N/A

Table 1-3. Equipment and Publications Required But Not Supplied

Category	Recommended equipment	Equipment test parameters	Application
Detector	Detector, Coaxial Crystal	Frequency Range: 0.1-26 Gz Frequency Response: ±1.5 dB from a 3.3 slope from 18 to 26 GHz Low Level Sensitivity >0.18 mV/ W to 26 GHz	Performance Test, Installation
Counter	Counter, Electronic Frequency	Frequency Range: 0.1-26 GHz Resolution: 100 kHz	Troubleshooting, Performance Test, Installation, Corrective Maintenance
Oscilloscope	Oscilloscope	Bandwidth: 100 MHz Input Sensitivity: 2 mV/division	Troubleshooting, Performance Test
Power Meter	Power Meter, Thermistor	Power Range: -20 dBm to +10 dBm Accuracy: ± 1% of full scale Frequency Range: 0.1 - 26 GHz	Troubleshooting, Performance Test Installation
Power Head	Power Sensor, Thermistor Mount	Frequency Range: 0.1 - 18 GHz	Performance Test Troubleshooting
Multimeter	Multimeter, Digital	Display: 3 1/2 digits Functions: Volts, Ohms, Amperes	Troubleshooting Alignment
Power Supply	Voltage Source, Precision	Output voltage: ± 3 V	Alignment

Table 1-3. Equipment and Publications Required But Not Supplied-Continued

Category	Recommended equipment	Equipment test parameters	Application
		Accuracy: ±0.01% Resolution: 100 μV	
Power Head	Power Sensor, Thermistor Mount	Frequency Range: 18-26 GHz	Performance Test Troubleshooting
Spectrum Analyzer	Spectrum Analyzer	Frequency Range: 0.1-26 GHz Amplitude Range: -40 to +20 dBm Spectral Resolution: 1 kHz to 3 MHz	Performance Test Troubleshooting, Installation, Corrective Maintenance
Function Generator	Function Generator	Function: Square wave Frequency Range: 100 Hz - 100 kHz	Maintenance Turn-On, Performance Test

Table 1-4. Field Changes

Change number	Nomenclature	Description

Table 1-5. Factory Changes

Change number	Nomenclature	Description

OPERATION

CHAPTER 2

OPERATION

2-1. INTRODUCTION. This chapter explains the intended function of the WJ-1204-1, describes typical applications, provides a summary of operator controls and indicators, and provides instructions on how to operate the WJ-1204-1 Synthesized Signal Generator.

2-2. UNIT FUNCTION. The WJ-1204-1 is intended for applications requiring multi-octave frequency coverage from a single portable unit. It provides a compact source of RF energy covering the frequency range from 100 MHz to 26 GHz. The WJ-1204-1 derives its RF output from a voltage-controlled oscillator, which provides the fundamental frequencies. Frequency doublers and a yttrium-iron garnet (YIG)-tuned multiplier provide the frequencies above 1 GHz. The instrument is capable of producing discrete, modulated, or swept signals.

2-3. Various units may be tested with the WJ-1204-1 including antennas, amplifiers, transmission lines, filters, attenuators, preselectors, isolators, switches, or combinations of components which make up a system. Typical applications are sensitivity measurements, insertion loss, frequency measurements, power measurements, and radar and receiver alignments. As shown in figure 2-1, insertion loss and gain measurements may be taken directly without the need for additional instruments by applying the output of the test device to the EXT RF IN connector. Gain or loss in dBm is deter-

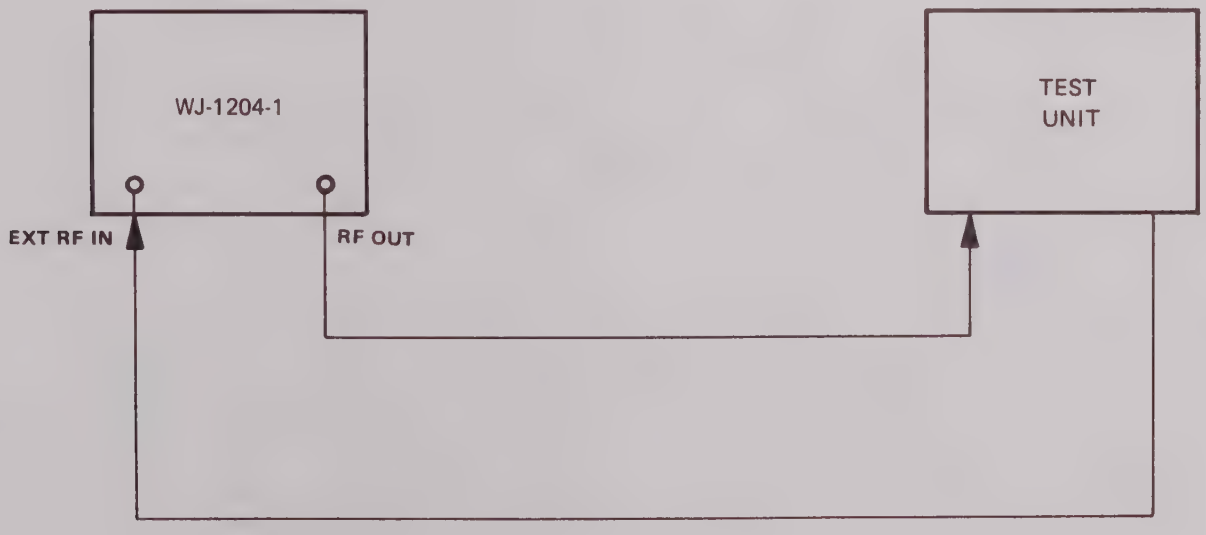


Figure 2-1. Typical Insertion Loss and Gain Measurement

mined at each frequency by taking the difference in the power levels as the unit is switched from the internal to external measurement mode. This capability is particularly useful during system check-out, when the gain of amplifiers and the insertion loss of the RF cables and other devices must be determined. Figure 2-2 shows a typical swept frequency set-up for measuring insertion loss, frequency response, return loss (VSWR), selectivity, and gain as a function of frequency. The MOD IN jack may be used in this application with network analyzers requiring modulation of the RF signal.

2-4. CONTROLS AND INDICATORS. The front and rear panel controls, connectors, and indicators are shown in figures 2-3 and 2-4. Table 2-1 lists all controls and indicators by name and functional description, and table 2-2 is a list and description of the front and rear panel connectors.

2-5. OPERATING PROCEDURES. The following paragraphs describe the operating procedures for the WJ-1204-1. The number in parentheses ( ) following a control name is a location identification number shown in figure 2-3.

2-6. Operator Turn-On. To turn on the WJ-1204-1, perform the steps listed in table 2- 3.

2-7. Modes of Operation. The Synthesized Signal Generator is capable of eight modes of operation which are described in table 2-4. Information on the remote operation of the unit is contained in the Users Note for WJ-1204-1 Option AB, General Purpose Interface Bus (GPIB), IEEESTD-488/1978 (Appendix A).

2-8. Operator Turn-Off. To turn off the unit, set the POWER switch (20, figure 2-3) to the OFF position.

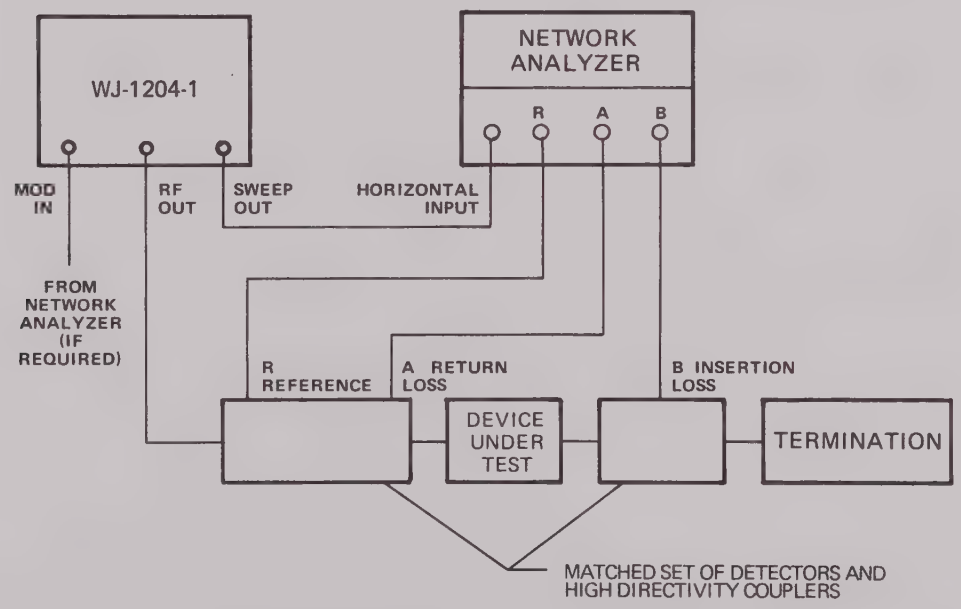
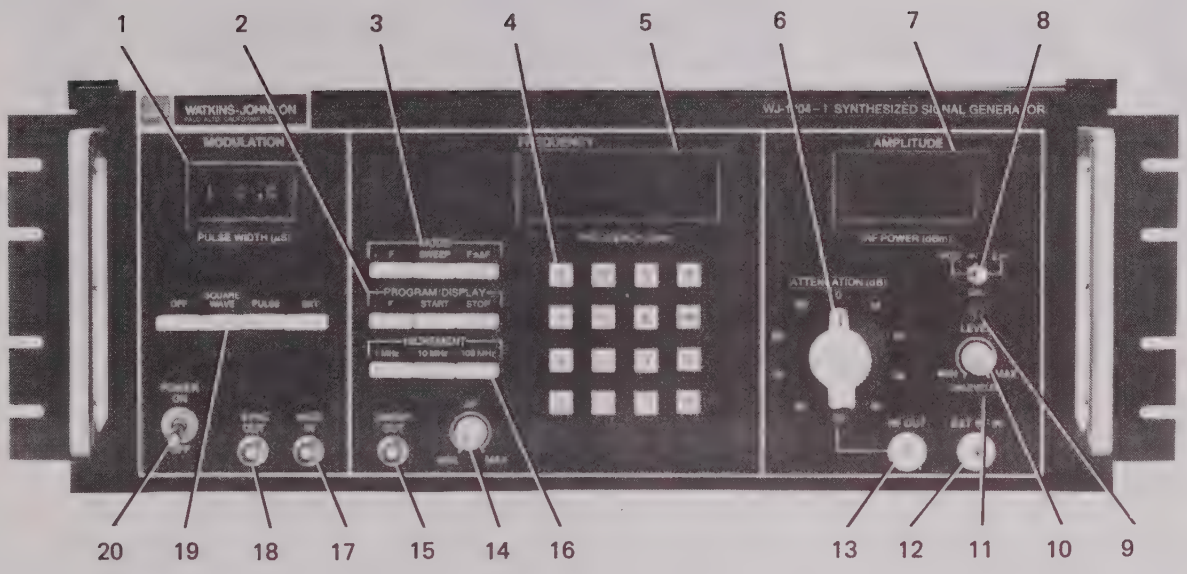


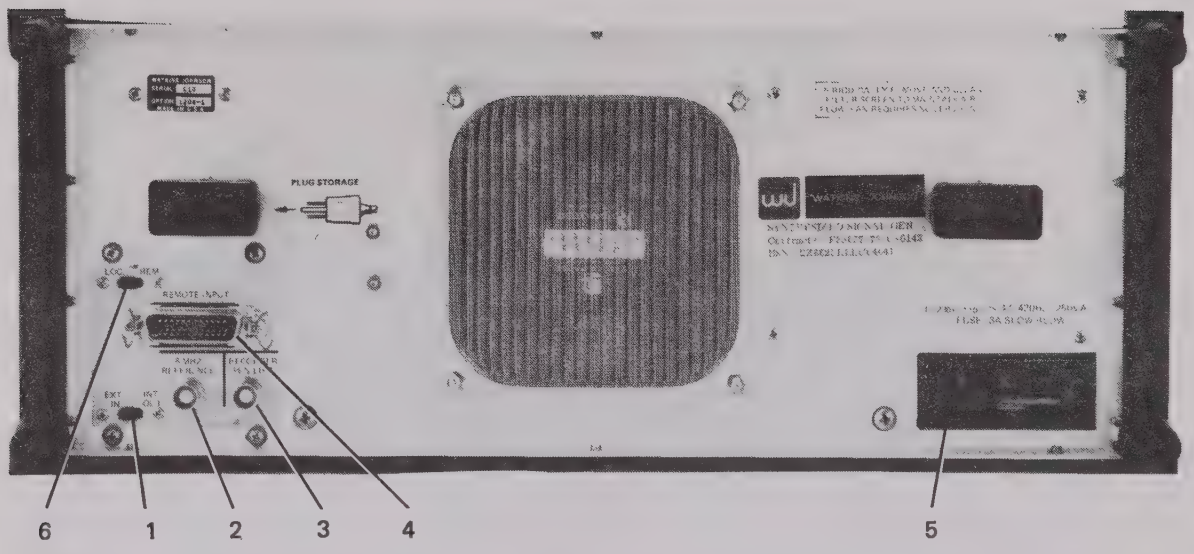
Figure 2-2. Typical WJ-1204-1/Network Analyzer Test Setup



79-H-563

1. PULSE WIDTH (μS) thumbwheel switches
2. PROGRAM DISPLAY pushbuttons
3. MODE pushbuttons
4. Keyboard
5. FREQUENCY (GHz) display
6. ATTENUATION (dB) selector
7. RF POWER (dBm) display
8. Power Meter Select switch
9. CAL pushbutton
10. LEVEL potentiometer
11. UNLEVELED indicator
12. EXT RF IN SMA connector
13. RF OUT SMA connector
14. ΔF potentiometer
15. SWEEP OUT BNC connector
16. INCREMENT pushbuttons
17. MOD IN BNC connector
18. SYNC OUT BNC connector
19. Modulation Select pushbuttons
20. POWER toggle switch

Figure 2-3. Front Panel Controls, Indicators, and Connectors



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1. 5 MHz REFERENCE select switch
2. 5 MHz REFERENCE I/O connector
3. RECORDER PEN LIFT connector
4. REMOTE INPUT connector
5. AC power input connector
6. Local/Remote select switch

Figure 2-4. Rear Panel Controls and Connector

Table 2-1. Controls and Indicators

Control/indicator	Ref des	Description
POWER (20, figure 2-3)	S1	Two-position toggle switch. In the ON position, power is applied to the unit. In the OFF position power is removed.
Modulation Selection Switches (19, figure 2-3)	S3	Four latching pushbutton switches. Select either square wave, pulse, or external modulation.
OFF	S3A	Turns off the modulation.
SQUARE WAVE	S3B	Modulates the RF signal with a 1 kHz square wave.

Table 2-1. Controls and Indicators-Continued

Control/indicator	Ref des	Description
PULSE	S3C	Modulates the RF signal with a pulse.
EXT	S3D	Permits the RF signal to be modulated by an external source.
PULSE WIDTH (μS) (1, figure 2-3)	S2	Three thumbwheel switches. They set the modulation pulse width from 00.1 to 10.0 microseconds in 0.1-microsecond increments.
MODE (3, figure 2-3)	S4	Three latching pushbutton switches. Used in conjunction with the keyboard to set the output frequency.
F	S4A	In this mode of operation the output of the signal generator is a single frequency as determined by the keyboard input.
SWEEP	S4B	This is a narrow to wide band stepped sweep mode. The output will automatically frequency step in the selected increment between the established frequency limits.
F $\pm$ ΔF	S4C	This is a narrowband continuous sweep mode. The output of the unit will deviate around the stabilized center frequency at a 1 kHz fixed rate. The desired sweep width (ΔF) is set with the ΔF potentiometer.
PROGRAM/DISPLAY (2, figure 2-3)	S5	Three latching pushbutton switches. Select the display and keyboard for entering the desired frequency.
F	S5A	Selects the keyboard to allow the desired frequency to be entered and displayed.
START	S5B	Selects the keyboard to allow the starting sweep frequency to be entered and displayed.
STOP	S5C	Selects the keyboard to allow the stop sweep frequency to be entered and displayed.
INCREMENT (16, figure 2-3)	S6	Three latching pushbutton switches. Select the desired sweep increments.

Table 2-1. Controls and Indicators-Continued

Control/indicator	Ref des	Description
1 MHz	S6B	Selects 1 MHz for the sweep increment.
10 MHz	S6C	Selects 10 MHz for the sweep increment.
100 MHz	S6A	Selects 100 MHz for the sweep increment.
ΔF(14, figure 2-3)	R1	Single-turn potentiometer. Adjusts sweep width in F ± ΔF mode.
FREQUENCY (GHz) (5, figure 2-3)	A1DS1 through A1DS5	Five-digit LED display. Displays the programmed frequency. The display will flash on and off if the programmed frequency is out of range. (The output frequency remains at the last correctly programmed frequency.) After an out-of-range frequency has been programmed, the CLR button must be pressed to clear the display and permit a new frequency to be programmed.
Keyboard (4, figure 2-3)		Sixteen-button switch matrix. When pressed, they load the selected frequency data (up to five digits) into the data bus and set the decimal point.
UP		When pressed, steps the frequency up. Keeping it pressed advances the frequency.
DWN (Down)		When pressed, steps the frequency down. Keeping it pressed decrements the frequency.
RST (Restart)		When pressed, it sets the output frequency to 1.0 GHz or, if in the sweep mode, to the start frequency.
ENT (Enter)		When pressed, it instructs the microprocessor to configure the unit to output the new frequency. If the new frequency is invalid, an error latch causes the display to flash.
CLR (Clear)		If a new frequency word has been keyed into the input but not entered, pressing CLR resets the display to the previously programmed frequency. If an invalid frequency has been entered, CLR must be pressed to clear the error condition.

Table 2-1. Controls and Indicators-Continued

Control/indicator	Ref des	Description
RF POWER (dBm) (7, figure 2-3)	A1DS6 through A1DS9	Three-digit plus sign LED display. Displays the RF power out in dBm. The display is blanked when in the internal or external modulation mode.
Power Meter Select (8, figure 2-3)	A1S1	Three-position toggle switch. In the EXT position, the EXT RF IN jack is connected and allows an external RF source to be applied to the power meter. In the INT position, the internal RF power is monitored and routed through the attenuator switch. The MOD position is a non-latching, spring-loaded position. Setting the switch to the MOD position turns off the modulation (if currently in that mode) and permits the continuous wave (CW) power to be shown on the RF POWER (dBm) display.
CAL (9, figure 2-3)	S15	Pushbutton switch. Pressing this switch causes the power detector to self-calibrate.
ATTENUATION (dB) (6, figure 2-3)	AT1	Ten-position rotary switch. Selects the level of RF output attenuation from 0 to 90 dB in 10 dB steps.
UNLEVELED (11, figure 2-3)	DS1	LED indicator. Lights when the RF output power is unleveled.
LEVEL (10, figure 2-3)	R2	Single-turn potentiometer. Allows an additional 0 to 20 dB attenuation in conjunction with the 0 to 90 dB attenuator.
5 MHz Reference Select (1, figure 2-4)	S13	Slide switch. The INT OUT position selects the internal 5 MHz reference oscillator; the EXT IN position allows an external 5 MHz reference to be applied to the Synthesizer Assembly via the BNC connector.
LOCAL/REMOTE (Option AB only)	S14	Slide switch. LOCAL position allows front panel control. REMOTE position allows computer control of frequency through REMOTE INPUT connector according to IEEE STD-488/1978.

Table 2-2. Front and Rear Panel Connectors

Connector	Ref des	Description
SYNC OUT (18, figure 2-3)	J1	BNC connector. Provides an external sync signal from the modulator.
MOD IN (17, figure 2-3)	J2	BNC connector. With the EXT modulation selector push-button switch pressed, an external modulating source may be applied.
SWEEP OUT (15, figure 2-3)	J3	BNC connector. With the mode switch in the F $\pm$ ΔF position, an external sync signal is provided from the ΔF sweep generator. In the wideband sweep mode, a voltage ramp proportional to frequency is provided.
RF OUT (13, figure 2-3)	J5	SMA connector. Provides the RF output of the WJ-1204-1.
EXT RF IN (12, figure 2-3)	J4	SMA connector. Provides a means for supplying an external RF signal to the WJ-1204-1. This connector is active when the MOD/INT/EXT switch is in the EXT position.
5 MHz REFERENCE (2, figure 2-4)	J7	BNC connector. With the 5 MHz Reference Select rear panel switch in the INT OUT position, a sample of the reference is available at this connector. With the switch in the EXT IN position, an external 5 MHz signal may be applied at this connector.
RECORDER PEN LIFT (3, figure 2-4)	J8	BNC connector. Outputs a voltage during a retrace (when in the sweep mode) to operate the z-axis of an x-y recorder.
REMOTE INPUT (Option AB only)	J10	24-Pin connector. Provides connection for GPIB bus (IEEE STD-488/1978).

Table 2-3. Turn-On Procedure

Step	Action
1	Select proper position of circuit card beneath fuse (i.e. for 115 or 230 volt ac operation).
2	Connect the WJ-1204-1 to a primary source (115 or 230 Vac).
3	Set POWER switch to the ON position. Allow a 10 to 15 minute warm-up period.
4	Press the CAL switch momentarily and then release it.
5	Connect a 50 ohm load to the RF OUT jack. The unit is now ready for operation.

Table 2-4. Operating Instructions

Operation to be performed	Procedure	Operational status
1. Entering discrete frequency	To create a single selected frequency, proceed as follows:	
	a. Perform turn-on procedure.	a. The unit powers up to 1.0000 GHz as displayed on the LED display.
	b. Press MODE F switch (3).	
	NOTE Numbers in parenthesis correspond to the location identification number shown in figure 2-3.	
	c. Press PROGRAM/DISPLAY F switch (2).	
	d. Program the desired frequency ($0.1 \leqslant f \leqslant 26$ GHz) on the keyboard.	d. The FREQUENCY (GHz) LED display shows programmed frequency.
	e. Press the ENT key on the keyboard.	e. The programmed frequency is now available at RF OUT connector.

Table 2-4. Operating Instructions-Continued

Operation to be performed	Procedure	Operational status
2. Entering sweep mode	To program the RF output to sweep between two set frequencies with a selected step, perform the following:	
	a. Perform turn-on procedure.	a. The unit powers up to 1.0000 GHz as displayed on the LED display.
	b. Press the MODE F switch (3).	
	c. Press the PROGRAM/DISPLAY START switch (2).	
	d. Program the starting sweep frequency on the keyboard.	d. The FREQUENCY (GHz) LED readout displays the start frequency.
	e. Press the ENT key on the keyboard.	e. The START frequency is internally loaded into the memory.
	f. Press the PROGRAM/DISPLAY STOP switch (2).	
	g. Program the stop sweep frequency on the keyboard.	g. The FREQUENCY (GHz) LED readout displays the stop frequency.
	h. Press the ENT key on the keyboard.	h. The STOP frequency is internally loaded into the memory.
	i. Press PROGRAM/DISPLAY F switch (2).	
	j. Select the desired sweep increment of 1 MHz, 10 MHz, or 100 MHz on the INCREMENT switch (16).	
	NOTE When none of the INCREMENT switches are pressed, the frequency will automatically increment in 100 kHz steps.	

Table 2-4. Operating Instructions-Continued

Operation to be performed	Procedure	Operational status
2. (Continued)	k. Press the MODE SWEEP switch (3). NOTE In order to avoid wearing out the mechanical switches, the following continuous sweep bands are allowable: 0.1 - 1.0 GHz 1.0 - 2.0 GHz 2.0 - 8.0 GHz 8.0 - 13.0 GHz 13.0 - 18.0 GHz 18.0 - 26.0 GHz If both the START and STOP sweep frequencies are within one of the above bands, the unit will continuously sweep within the programmed limits. If the sweep limits straddle one or more band edges, the unit will stop at the band edge and flash the frequency display. The operator may continue the sweep by pressing the ENT button on the keyboard. l. To program a different set of stop/start frequencies, press the MODE F switch and repeat steps c through k above. NOTE If the stop frequency is lower than the start frequency, the unit will sweep down.	k. The RF output is sweeping as displayed on the LED readout.
3. Entering $F \pm \Delta F$ mode	To program the RF output to vary about a center frequency, perform the following:	

Table 2-4. Operating Instructions-Continued

Operation to be performed	Procedure	Operational status
3. (Continued)	a. Perform turn-on procedure.	
	b. Press the PROGRAM/DISPLAY F switch (2).	
	c. Press the MODE F switch (3).	
	d. Program the desired center frequency on the keyboard.	d. The center frequency is displayed.
	e. Press the ENT key on the keyboard.	e. The center frequency is now available at the RF OUT connector.
	f. Press the MODE F $\pm\Delta$F switch (3).	
	g. Rotate the ΔF control (14) to the desired sweep width.	g. The RF output is now varying about the center frequency at a 1 kHz rate.
	NOTE Frequency may be slewed up or down with the UP or DWN pushbuttons while in this mode.	
4. Square wave modulation	To program the RF output for square wave modulation, perform the following:	
	a. Enter the frequency to be modulated as described in step 1 above.	
	b. Press the SQUARE WAVE switch (19).	b. The RF output is now modulated with a 1 kHz square wave.
5. Pulse modulation	To program the RF output for pulse modulation, perform the following:	
	a. Enter the frequency to be modulated as described in step 1 above.	a. FREQUENCY display shows programmed frequency.

Table 2-4. Operating Instructions-Continued

Operation to be performed	Procedure	Operational status
	b. Set the PULSE WIDTH (μS) thumbwheel switches (1) to the desired parameters.	
	c. Press the PULSE switch (19).	c. The RF output is now pulse-modulated with a pulse repetition rate of 1 kHz.
6. External modulation	To modulate the RF output with an external source, perform the following:	
	a. Enter the frequency to be modulated as described in step 1 above.	a. FREQUENCY display shows programmed frequency.
	b. Apply the external modulation signal to the MOD IN jack (17).	
	c. Press the EXT switch (19).	c. The RF output is now externally modulated.
7. Setting RF amplitude	To set the amplitude of the RF output signal, perform the following:	
	a. Enter a frequency as described in step 1 above.	a. FREQUENCY display shows programmed frequency.
	b. Set the ATTENUATION (dB) control (6) to the desired 10 dB step attenuation.	b. The unattenuated RF output power will be displayed on the RF POWER (dBm) LED display.
	c. For further adjustment of the attenuation level, turn the LEVEL control (10) to the desired setting. In the	c. The RF POWER (dBm) readout will display the attenuated RF power as set by the LEVEL control. (The display

Table 2-4. Operating Instructions-Continued

Operation to be performed	Procedure	Operational status
7. (Continued)	MIN position, approximately 20 dB of additional attenuation is provided; in the MAX position, no additional attenuation is provided. NOTE The RF POWER (dBm) display is blanked during SQUARE WAVE, PULSE, and EXT modulation modes. Because the internal detector measures average power only, measure the level of the "on" portion of the modulated signal by setting the Power Meter Select switch momentarily to the MOD position and read the display. When the Power Meter Select switch is held in the MOD position, the modulation is removed from the signal which becomes a cw signal at the level of the "on" portion of the modulated signal and the power meter display is unblanked.	will not show the 0-90 dB attenuation steps selected.)
8. Measuring external RF power	To measure the power of an external RF signal, perform the following: CAUTION The maximum input power to the detector must not exceed +15 dBm (31.6 mW). a. Apply the external RF to the EXT RF IN connector (12). b. Place the Power Meter Select switch (8) to the EXT position. c. Set POWER switch (20) to ON.	c. The external RF power will be displayed on the LED readout.

CHAPTER 3

FUNCTIONAL DESCRIPTION

3-1. INTRODUCTION. This chapter provides a general and detailed theory of operation for the WJ-1204-1 Synthesized Signal Generator. An overall block diagram is included. Schematic diagrams for all circuit cards described are provided in chapter 5, component location diagrams are provided in chapter 7.

3-2. FUNCTIONAL ANALYSIS. The WJ-1204-1 is programmed manually from the front control panel. It is capable of providing a spectrally pure output signal by phase-locking a voltage controlled oscillator (VCO) to an internal or external 5 MHz reference.

3-3. Figure 3-1 is an overall block diagram and figure 5-1 is a detailed schematic diagram of the WJ-1204-1 Synthesized Signal Generator. The general theory of operation follows.

3-4. Frequency commands entered by the operator at the keyboard are processed by Digital Control and Remote Interface Circuit Card Assembly A5. This assembly translates keyboard commands into the proper format to control the switching of RF signals and provide the proper coarse-tune voltage to the VCO. Frequency accuracy is determined by a 5 MHz signal from either an internal 5 MHz crystal oscillator or an externally applied 5 MHz reference. The 5 MHz signal is programmably divided to one of three frequencies, 10 kHz, 12.5 kHz, or 7.8125 kHz. The output signal from VCO Y1 is also programmably divided to obtain the same frequencies. These two frequencies are applied to a phase detector. The detector output consists of a fine-tune voltage which is then applied to the VCO, thus closing the phase lock loop.

NOTE

If the ΔF mode has been selected, the correction voltage to the VCO will be modulated by the ΔF frequency generator.

3-5. The output of Y1 goes through directional coupler CP4 and is divided by Power Splitter A8. The coupled output is applied directly to Pin Leveler/Switch S7, and both outputs from A8 are applied to the prescaler on Synthesizer Circuit Card Assembly A7. Prescaler outputs are applied to S7 and to the programmable divide-by-N circuit on A7. The output from S7 is applied through Pulse Modulator A9 to Low Frequency Switch/Filter Assembly A10. To obtain the frequencies that are above 1 GHz, part of the output from A10 is multiplied by 2 and applied to another Switch/Filter Assembly, A12. If the selected frequency is between 1 and 2 GHz the output from A12 is fed to Coaxial RF Switch Assembly S10. If the selected frequency is higher than 2 GHz the output from A12 is applied to yttrium-iron garnet (YIG)-tuned multiplier A13. The YIG-tuned multiplier is tuned by the microprocessor to the second, fourth, or eighth harmonic of the input signal. The output of the YIG-tuned multiplier is applied to Pin Leveler A14 which sets the RF output level. The output of A14 is applied to switch S8.

3-6. If the selected frequency is 2 to 8 GHz, the output of S8 is applied to switch S10. If the selected frequency is above 8 GHz, the output of S8 is applied to traveling

wave tube amplifier (TWTA) AR3. The output of AR3 is applied to switch S9. If the selected frequency is 8 to 13 GHz, the signal is passed through a low pass filter and then to S10. If the selected frequency is 13 to 18 GHz, the frequency is first doubled by A17 and then applied to switch S10. If the selected frequency is 18 to 26 GHz, the frequency is first doubled by A16 and then applied to switch S11.

3-7. Switch S10 selects one of four frequency bands between 1 and 18 GHz. This output is applied to switch S11. The selected frequency from S10 is also directionally coupled to switch S12. Switch S12 selects the frequency range being used and applies it to Power Detector A15 for monitoring. The RF power sampled by A15 is converted into an equivalent dc voltage by Power Meter Circuit Card Assembly A3. This voltage drives the power display through an analog-to-digital converter. A3 also supplies an input to the leveling circuitry on RF Control Circuit Card Assembly A4 to drive the PIN attenuator in S7 and A14.

3-8. Switch S11 selects one of three frequency ranges (18 to 26 GHz, 1 to 18 GHz, or 0.1 to 1 GHz) for input to the final Step Attenuator AT1. This attenuator (ATTENUATION (dB) switch on the front panel) adjusts the RF output to the desired level.

3-9. DETAILED CIRCUIT ANALYSIS. The following paragraphs provide a detailed analysis of each circuit card assembly (CCA) within the WJ-1204-1 Synthesized Signal Generator. Each description is referenced to the appropriate schematic diagram and supported, where necessary, with simplified block diagrams.

3-10. DIGITAL CONTROL AND REMOTE INTERFACE A5. Digital Control and Remote Interface A5 (figure 5-5) is a microprocessor-based system built around the Z-80 CPU (central processing unit) which is a third generation microprocessor using n-channel metal-oxide semiconductor (MOS) technology. The Z-80 CPU is designed to work directly with a minimum number of memory and peripheral support chips, a single +5 volt supply, and a single-phase clock. The clock frequency of approximately 2 MHz permits instructions to be executed in 2 to 9 microseconds.

3-11. As in any microprocessor-based system, the circuitry of A5 consists of a CPU, a random access memory (RAM) for temporary storage of data, a read-only memory (ROM) for storing the system's program parameters, and a set of input/output (I/O) interface chips. (See figure 3-2.)

3-12. Central Processing Unit. CPU U4 is the heart of the system. Its function is to obtain (fetch) instructions from memory and perform the desired mathematical, logical, or transfer operation. The CPU is designed around the popular parallel data bus concept so that all memory and peripheral interface chips simply hang on the CPUs eight bi-directional data lines. Inside the CPU are eighteen 8-bit registers and four 16-bit registers. All CPU registers are implemented by static RAM. The CPU uses a single-phase clock generated by voltage-controlled multivibrator U3 which times various CPU functions. The clock is factory set for a frequency of approximately 2 MHz.

3-13. Various control signals are generated by the CPU to dictate the use of the board's 8-bit data bus for data input/output, program memory input, or random-access memory. Ordinarily, the Z-80 CPU takes six control inputs and generates eight control outputs as listed in table 3-1. Some of these are not used in this application and are so indicated in the table.

3-14. Memory. The memory of this microprocessor-based system is both RAM and ROM. There are 256 bytes of RAM. Circuits U18 and U19 are used for scratch-pad logic control and general purpose storage of data. U19 holds the least significant nibble (LSN) and U18 the most significant nibble (MSN) of each byte of RAM. (One nibble = 4 bits = 1/2 byte.)

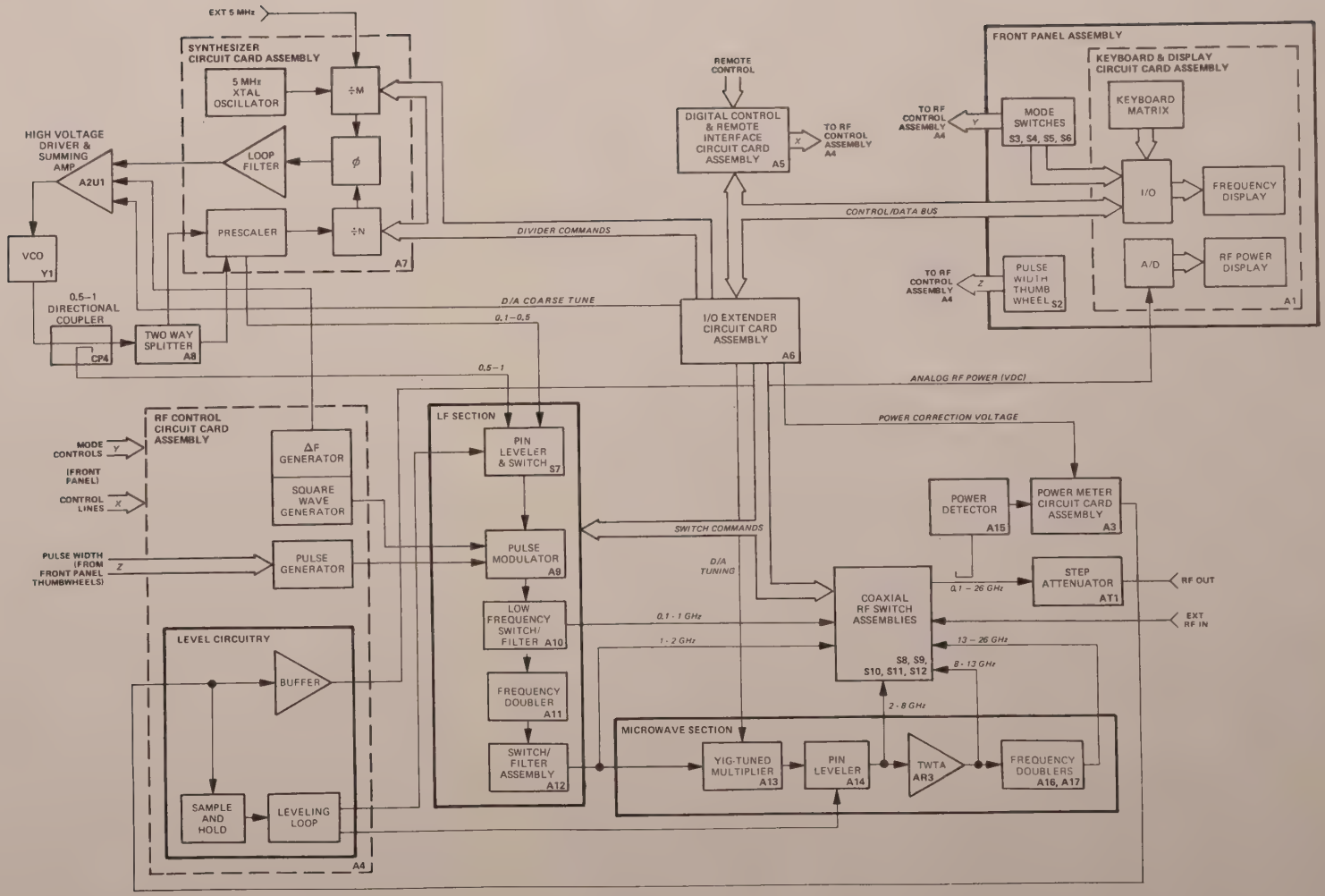

Figure 3-1. WJ-1204-1 System Block Diagram

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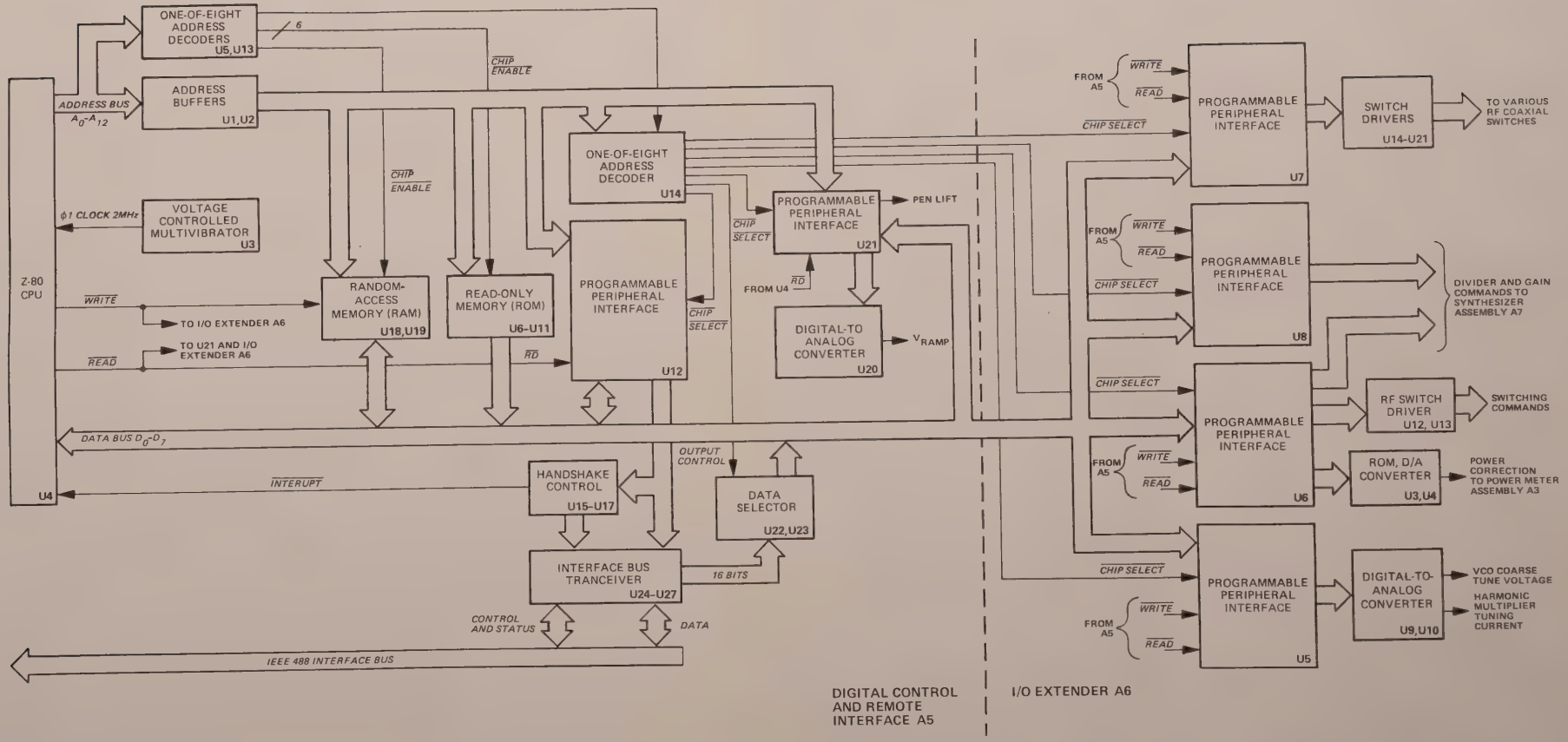


Figure 3-2. Digital Control and Remote Interface A5, and I/O Extender A6, Block Diagram

78-L-048

Table 3-1. CPU I/O Lines

Control	Description
A_0 through A_{15}	Output. A 16-bit address which defines a memory or input/output port location.
D_0 - D_7	Input/output. Tri-state active high bidirectional data bus.
$\overline{HALT}$	Output. A negative-true line that indicates the CPU has executed a $\overline{HALT}$ software instruction and is awaiting either an $\overline{INT}$ or $\overline{NMI}$ input. (Not used in this configuration.)
$\overline{IORQ}$ (Input/Output Request)	Output. A negative-true line which indicates the address lines and data bus are being used for an input or output operation on a peripheral device. (Not used in this configuration.)
$\overline{MREQ}$ (Memory Request)	Output. A negative-true line which indicates the address lines and data bus are being used for memory input or output.
$\overline{M1}$ (Machine Cycle One)	Output. A timing signal which indicates the CPU is in an operation (op) code fetch-mode of operation. This is the first of two to sixteen machine cycles which comprise a complete instruction cycle for the CPU. (Not used in this configuration.)
$\overline{BUSAK}$ (Bus Acknowledge)	Output. A negative-true signal that indicates to the requesting device that the CPU can now be controlled by the external device. (Not used in this configuration.)
$\overline{RD}$ (Memory Read)	Output. A negative-true signal which indicates that the data bus is being used as an input to the CPU.
$\overline{RFSH}$ (Refresh)	Output. A negative-true line that indicates the address lines are being used to refresh dynamic RAM. (This signal is not necessary for use by the static RAM. Thus, it is used to disable any memory selection by one-of-eight decoder U5.)
$\overline{WR}$ (Memory Write)	Output. A negative-true line that indicates the CPU is using the address lines and data bus to write data into memory for storage purposes.
$\overline{BUSRQ}$ (Bus Request)	Input. A negative-true line that disables the CPU's use of the data bus. (Not used in this configuration.)

Table 3-1. CPU I/O Lines-Continued

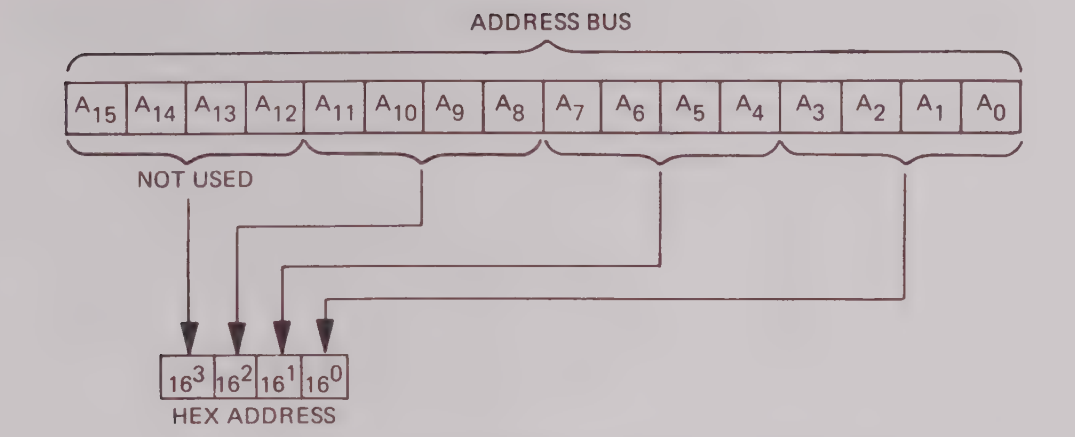
Control	Description
Φ (Clock)	Input. CPU clock input (approximately 2 MHz).
$\overline{INT}$ (Interrupt Request)	Input. A firmware maskable interrupt used by the peripheral devices to stop normal operation of the CPU and service the peripheral device.
$\overline{RESET}$	Input. A negative-true line that forces the program counter to zero and initializes the CPU. (Not used in this configuration.)
$\overline{WAIT}$	Input. A negative-true signal that suspends all CPU activity. (Not used in this configuration.)
$\overline{NMI}$ (Non-Maskable Interrupt)	Input. A negative-edge triggered interrupt request line that has higher priority than $\overline{INT}$. (Not used in this configuration.)

3-15. The second kind of memory is the ROM. Circuits U6 through U11 are programmable ROMs (PROMs) and are used principally to store programmed instructions and non-volatile data constants that will be fetched as operands while the CPU executes a program. In a microprocessor-based system, circuit functions are determined by a program (a sequence of instructions) stored in the PROM. Therefore, replacing the program can completely alter the function of the equipment that contains the microprocessor. This aspect of a microprocessor-based system makes it easier to modify or upgrade the system.

3-16. There are sockets for up to 3,000 bytes of program memory on the board. Address bus decoders U5 and U13 are one-of-eight decoders which select memory address locations. This is done by decoding address lines A_8 through A_{12} into an active-low chip enable ($\overline{CE}$) output which allows only one RAM or PROM to put data on the data bus. When the Y4 output of U13 goes low, for example, both RAMs U18 and U19 are selected. Figure 3-3 shows how the microprocessor address lines select a memory or I/O device. Address locations of all addressable devices are also shown in figure 3-3. There are 56 bits of memory-mapped I/O (seven bytes).

3-17. I/O Interface Circuits. To do anything useful, any processor, micro or otherwise, must have one or more I/O devices connected to it so that it can acquire data to process and then dispose of the results. The interface circuits on A5 are of two types: programmable I/O and dedicated I/O. Address decoder U14 controls which of these circuits is enabled to input or output to the CPU. This is done by decoding address lines A_2 through A_4, when A_8 through A_{11} are all high.

3-18. The programmable I/O circuits consist of U12 and U21. These are Programmable Peripheral Interface (PPI) integrated circuits (ICs) which have software programmable I/O functions. Immediately after power is applied to the WJ-1204, these ICs receive mode of operation commands from



	IC ENABLED	HEXADECIMAL ADDRESS LOCATION FROM 16^3	16^2	16^1	16^0	TO 16^3	16^2	16^1	16^0	
DIGITAL CONTROL & REMOTE INTERFACE A5	U18, U19	X	E	0	0	X	E	F	F	RAM
	U6	X	0	0	0	X	1	F	F	ROM
	U7	X	2	0	0	X	3	F	F	
	U8	X	4	0	0	X	5	F	F	
	U9	X	6	0	0	X	7	F	F	
	U10	X	8	0	0	X	9	F	F	
	U11	X	A	0	0	X	B	F	F	
	U12	X	F	0	4	X	F	0	7	
	U21	X	F	0	0	X	F	0	3	
	U22, U23	X	F	0	8	X	F	0	9	
I/O EXTENDER A6	U5	X	F	1	8	X	F	1	B	I/O
	U6	X	F	1	4	X	F	1	7	
	U7	X	F	0	C	X	F	0	F	
	U8	X	F	1	0	X	F	1	3	
KEYBOARD & DISPLAY A1	U1, U2, U9	X	C	0	0	X	C	0	7	

X = DON'T CARE

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Figure 3-3. CPU Address Allocations

the CPU (i.e. which of their I/O ports are to be used for input or output). PPI U12 interfaces the CPU with a remote device, and U21 provides digital-to-analog converter (D/A) U20 with digital information. U20 then converts the digital input to the equivalent analog output voltage (Vramp) (see table 3-2). Address lines A_0 and A_1, and inputs $\overline{RD}$ and $\overline{WR}$, are the control inputs that select one of the three ports to interface with the data bus (see table 3-3).

3-19. Of the three possible modes of operation that are software selectable, both U12 and U21 are programmed (during the unit power-up cycle) to operate in Mode 0. This mode, or functional configuration, provides simple input and output operations for each of the three ports. No handshaking is required in this mode; data is simply written into or read from a specified port. Functionally speaking then, both PPIs can be thought of as RAMs. Figure 3-4 illustrates

Table 3-2. D/A Converter A5U20 I/O

Analog output	Sign bit	Input pins MSB 1	2	3	4	5	6	7	8	9	LSB 10
+ FULL SCALE	1	1	1	1	1	1	1	1	1	1	1
+ HALF SCALE	1	1	0	0	0	0	0	0	0	0	0
ZERO SCALE (+)	1	0	0	0	0	0	0	0	0	0	0
ZERO SCALE (-)	0	0	0	0	0	0	0	0	0	0	0
- HALF SCALE	0	1	0	0	0	0	0	0	0	0	0
- FULL SCALE	0	1	1	1	1	1	1	1	1	1	1

Table 3-3. PPI Control Inputs

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Functional Configuration	
0	0	0	1	0	PORT A to DATA BUS	Input Operation (READ)
0	1	0	1	0	PORT B to DATA BUS	
1	0	0	1	0	PORT C to DATA BUS	
0	0	1	0	0	DATA BUS to PORT A	Output Operation (WRITE)
0	1	1	0	0	DATA BUS to PORT B	
1	0	1	0	0	DATA BUS to PORT C	
1	1	1	0	0	DATA BUS to CONTROL	
X	X	X	X	1	DATA BUS to 3-STATE	Disable Function
1	1	0	1	0	ILLEGAL CONDITION	
X	X	1	1	0	DATA BUS to 3-STATE	

X = don't care

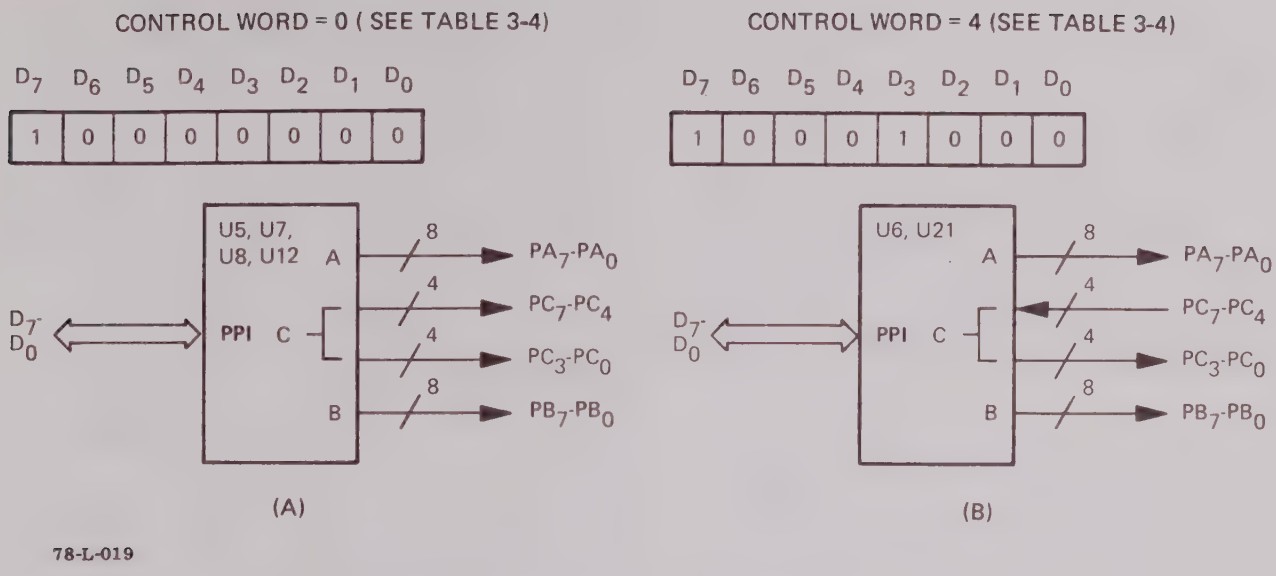


Figure 3-4. Mode O I/O Configuration

the specific I/O configuration for U12 and U21 and shows the control word output by the CPU to acheive this mode. A summary of the possible configurations of this mode is listed in table 3-4.

3-20. The dedicated I/O circuit is used to interface with a remote device. This circuitry (not included in some models of the WJ-1204-1) consists of the following:

U22, U23	Tri-state data selectors used to monitor interface bus commands and input the interface bus data lines to the unit.
U24 thru U27	Interface bus transmitter/ receivers used to communicate data and commands with the remote device.

Table 3-4. Summary of Possible Mode 0 Input/Output Configurations

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	Port A	Port C (upper)	Control Word	Port B	Port C (lower)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT

Table 3-4. Summary of Possible Mode 0 Input/Output Configurations - Continued

A		B		GROUP A		Control Word	GROUP B	
D_4	D_3	D_1	D_0	Port A	Port C (upper)		Port B	Port C (lower)
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

Note: D_2, D_5, and D_6 = 0, and D_7 = 1.

U15 One-shots used to generate interrupts to the CPU for quick reaction to an interface bus command of ATN (attention) or IFC (interface clear). Because it is difficult for the CPU to reliably detect certain peripheral status signals shorter than 10 microseconds (such as ATN or IFC), these one-shots widen the pulse so that the CPU can react to them.

U16, U1 NAND gates used to disable any interface bus transmission when ATN or IFC is sensed by the one-shots.

3-21. I/O EXTENDER CCA A6. As the name implies, this circuit is an extension of the Digital Control and Remote Interface, A5 (see figure 3-2). All PPI chips, U5 through U8 are programmed to receive data from the data bus and transfer it to its output ports. (A fuller description of the PPI chips is given in paragraph 3-17.) Figure

5-6 is a logic diagram of A6. When addressed, each PPI supplies control outputs to various circuits as summarized in figure 3-2.

3-22. SYNTHESIZER CCA A7. The Synthesizer assembly (figure 5-7) contains the phase and frequency locking circuitry that maintains the unit's stable and accurate RF frequency output. It consists of two programmable decade divider circuits (divide-by-M and divide-by-N), a divide-by-8 prescaler, a clock oscillator, a phase detector, and a loop filter. A block diagram of A7 is shown in figure 3-1.

3-23. A signal in the 0.5 to 1 GHz frequency range (VCO output) is applied to three divide-by-2 prescalers (U1, U2, and U3) that collectively constitutes a divide-by-8 prescaler. Each divide-by-2 IC not only feeds the next, but also outputs the resulting frequency to connectors J2, J3, and J4. The final output from U3 is in the range of 62.5 to 125 MHz, but only the 100 to 125 MHz portion is actually used. The VCO output is also applied to a divide-by-N circuit, which consists of decade counters U5 through U9 and divide-by-10, divide-by-11 prescaler U10. The counters will divide by any number from 20,000 to 64,000 depending on what program is supplied by the data bus. The divide-by-N circuit will always divide so that the final IF frequency out of U11B is either 10 kHz, 7.8125 kHz, or 12.5 kHz. The final IF is 10 kHz when the programmed frequency is 100 to 250 MHz, inclusive; 12.5 kHz when 0.25 to 2 GHz, inclusive; and 7.8125 kHz when greater than 2 GHz.

3-24. A 5 MHz reference is supplied by clock oscillator U20; an external 5 MHz reference may be input at connector J5. These two signals are applied to analog switch U19. The selected 5 MHz reference is applied to the divide-by-M circuit which consists of divide-by-10, divide-by-11 prescaler U13 and programmable decade counters U15 through U17. These counters are programmed by the data bus to divide the 5 MHz signal by 400, 500, or 640 so that the final output from U14C is either 10 kHz, 7.8125 kHz, or 12.5 kHz. This output is phase-compared with the output from U11B at phase detector U18. U18 determines the lead or lag phase relationship and the time difference between the leading edges of the two IF frequencies. The digital phase error information is supplied to integrator amplifiers AR1, AR2, and AR4. Analog switches U21 and U22 control the gain of amplifier AR2 by switching in various resistors determined by the CPU.

3-25. RF CONTROL CCA A4. The RF Control (figure 5-4) contains the automatic leveling control (ALC) circuitry, the pulse modulation and selection circuitry, the sample and hold circuitry, and the ΔF frequency generator of the WJ-1204-1. The mode of modulation is selected by an interlocked set of front panel switches (19, figure 2-3). When the switch assembly is in a position other than OFF, a logic 0 is applied to the corresponding U1 OR gate (U1-C for SQUARE WAVE, U1-A for PULSE, or U1-D for EXTERNAL modulation). This same logic 0 is also applied to AND gate U3-A or U3-C forcing the output of U3-C to its low state. This low level at pin 8 of U3 is applied to pins 16 and 9 of analog switch U8 which cause D15-S15 and D17-S17 to close. The output of U3-C is also inverted by U9-E which in turn forces the output of U1-B to go high. This high level signal opens switch D16-S16 because one-shot U19-A has not been triggered. Switch D18-S18 is also kept open by the high level output of U9-E because the output of U2-B remains high. The simultaneous opening of the switches D16-S16 and D18-S18 opens the leveling loop of the WJ-1204-1 because it removes the power meter input (pin 30) from the loop drivers. The closing of switch D17-S17 switches the front panel LEVEL control potentiometer from the input of high gain stage AR1-B to the input of low gain stage AR3-B. This adds stability in the open loop mode. The closing of switch D15-S15 shorts out resistor R33 and changes the voltage applied to the bottom of the LEVEL control from approximately -2.5 Vdc to -6.1 Vdc.

Control of the output power level is now achievable (in the open loop mode) by adjustment of the LEVEL control. When either the SQUARE WAVE or PULSE modulation pushbutton is pressed, a high level signal is applied to pin 9 of function generator U15. A 1 kHz square wave is output on pin 11 of U15 and applied to the base of driver transistor Q1. (Potentiometer R46 adjusts the frequency of this signal). The square wave also leaves the board on pin 14 and serves as the Modulation Sync ouput. Transistor Q1 inverts the square wave and applies it to one of the triggering inputs of one-shot U4. It is also applied to the base of inverting transistor Q6. In the square wave modulation mode, the output of U1-C causes switch D11-S11 to close, allowing the square wave to be applied to inverting buffer-driver U9-D. This square wave then leaves the board on pin 13 where it is applied to the pulse modulator. Note that U4 is prevented from triggering by the low level signal on pin 10. In the pulse modulation mode, the low output of U1-A closes switch D12-S12 and the high output of U9-C enables U4. The square wave at the collector of Q1 triggers U4 at a 1 kHz rate and the output of U4 is passed through the contacts of D12-S12 to buffer-driver U9-D where it is applied to the pulse modulator. The pulse width is controlled by a front panel thumbwheel switch which serves as the timing resistor for U4. Pulse widths are adjustable from 100 nanoseconds to 19.9 microseconds in 100 nanosecond increments. In the external modulation mode, the low output of U1-D closes switch D13-S13. This allows an external modulation signal to control the pulse modulator via the front panel BNC connector, pin 24 of the board, and the closed contacts of D13-S13. Zener diode VR-4 is present to protect inverter U9-D from excessive voltage.

3-26. The sample and hold circuitry consists of one-shots U19-A and U19-B, OR gates U1-B, U2-A, U2-B, U2-C, AND gates U3-B and U3-D, inverters U9-A and U9-B, dual clock U6, and analog switches U8 and U18-A as well as up/down counters U11, U12, and U14, digital-to-analog (D/A) converter U13, and comparator AR2-A. This circuitry is used to maintain the power level of the RF output when the power meter is being used in the external measurement mode. When the MOD-INT-EXT switch on the front panel is placed in the EXT position, a high level signal is applied to pin 2 of U19-A, pin 1 of analog switch U5, and pin 1 of OR gate U1-B. The high level signal at pin 1 of U5 opens the analog switch which removes a 1 volt bias from display driver AR1-A. This action is necessay because the external RF signal is applied directly to the power meter as opposed to the internal RF signal which passes through a 10 dB directional coupler. The log output voltage from the power meter has a slope of 10 dB per volt and removing this 1 volt bias allows the display to read the proper power level in the external mode. Refer to the timing diagram (figure 3-5) to aid in understanding the operation of the rest of the circuit. The high level signal at pin 2 of U19 triggers one-shot U19-A for approximately 12 milliseconds. The normally high $\overline{Q}$ output at pin 4 goes low triggering U19-B and keeping analog switch D16-S16 closed and switch D18-S18 open. This is the sample time. One-shot U19-B then triggers for approximately 5 milliseconds. The normally high ($\overline{Q}$) output of U19-B is used to enable the high frequency section of dual clock U6. The output appears as a 100 kHz signal at pin 7 of U6 where it passes through analog switch U18-A. This signal is used as the CP input for up/down counters U11, U12, and U14. After U19-B times out, the normally low (Q) output at pin 5 returns to its low state forcing the output of U2-C to be low which enables the low frequency section of U6. A 2 kHz signal appears on pin 10 of U6 which is coupled through analog switch U18-A to the CP inputs of U11, U12, and U14. When U19-A finally times out, the normally high output ($\overline{Q}$) returns to its high state opening analog switch D16-S16 and closing switch D18-S18. This removes the power meter voltage from the leveling loop and substitutes the output of D/A converter U13. During the sample time of approximately 12

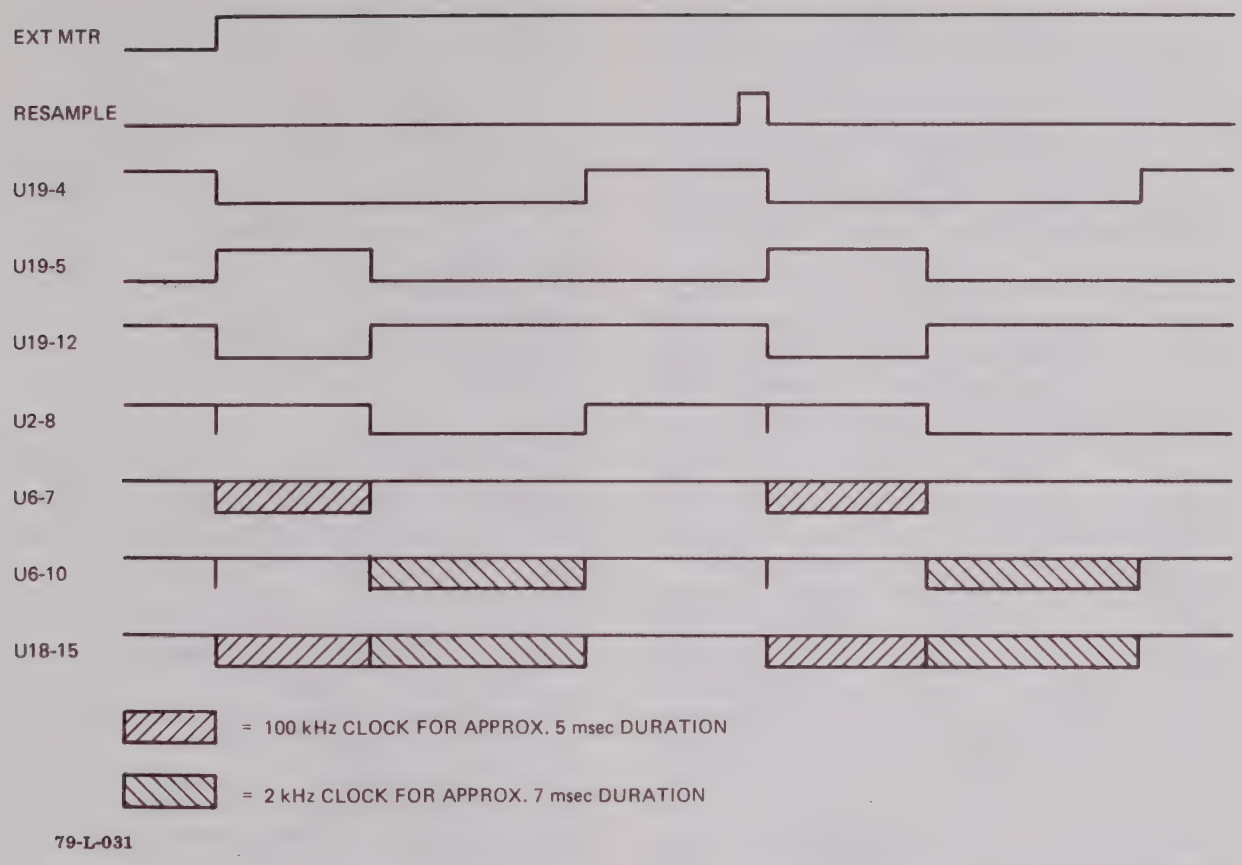


Figure 3-5. Timing Diagram For Sample and Hold

milliseconds, up/down counters U11, U12, and U14 are being clocked by the outputs of U6. These counters are arranged in a cascade configuration with their outputs being applied to the control inputs of U13. Comparator AR2-A is used to compare the power meter voltage (on R6) with the D/A output voltage (on R8). The comparator output controls the up/down function of counters U11, U12, and U14. D/A converter U13 will slew upward until the voltage at R8 exceeds the voltage at R6. This forces the comparator output low causing the counters (and thus the D/A) to slew down. The D/A output voltage will oscillate $\pm$ 1 LSB (least significant bit) about the power meter voltage until U19-A times out and the sample time ends. The circuit then goes into the hold mode with the D/A output voltage applied through D18-S18 to the input of AR3-B. The dual clock is provided to ensure that the D/A output slews quickly toward the power meter voltage at first but then oscillate slowly about the required value for accuracy. During the sample time the $\overline{Q}$ output of U19-A also forces AND gate U3-B to go low, which in turn zeros Power Meter CCA A3. The normally low output of U19-A removes any modulation from the pulse modulator during the sample time (in case the unit happens to be in one of the modulation modes). Once in the external measurement mode, a change of frequency using the ENT pushbutton will cause a pulse to appear on pin 1 of U19-A thus initiating the entire sample sequence again. This enables the unit to maintain a levelled output at different frequencies.

3-27. The ΔF frequency generator consists of U15 and its associated circuitry as well as analog switch D20-S20. U15 is a monolithic function generator which provides the triangular voltage used in the F ± ΔF mode as well as the 1 kHz square wave used in the modulated modes. Potentiometer R46 is adjusted to provide a nominal 1 kHz output frequency, and potentiometer R3 controls the amplitude of the triangle output. When the front panel F ± ΔF mode switch is pressed, pin 9 of U15 is forced high turning on the function generator. The triangular output, used for frequency modulating the VCO, appears on pin 2 of U15. This output is ac coupled through capacitor C21 to the front panel ΔF amplitude control and then to Synthesizer CCA A7. The triangular waveform is also applied to analog switch input D20. A 1 kHz square wave originating from pin 11 of U15 causes switch D20-S20 to open and close at a 1 kHz rate effectively chopping off one-half of the triangle output. The resulting sawtooth waveform is used as the ΔF Sync ramp and leaves the board on pin 16.

3-28. The leveling loop circuitry consists of operational amplifiers AR1-B, AR1-C, AR1-D, AR3-A, AR3-B, AR3-C, transistors Q2, Q3, and Q4, and their associated circuitry. The RF power level is converted to a dc voltage by Power Meter CCA A3 and applied to the inverting input of AR1-B. The front panel LEVEL control is connected to the non-inverting input and the output of AR1-B is applied through the normally closed contacts of D16-S16 to adjustment amplifier AR3-B. Potentiometers R78 and R114 are adjusted so that the current outputs of this assembly are a close match to the currents required by PIN Diode Leveler A14 (on RF deck). The output of AR3-B drives logarithmic correction amplifier AR1-C and driver amplifier AR1-D. The output of AR1-C is applied to driver amplifier AR3-A. Amplifier AR3-A and transistor Q2 control the series current applied to the leveler, and amplifier AR1-D and transistor Q3 control the total currents (series plus shunt). The entire circuit is designed to match the current vs attenuation characteristics of the leveling device. At output frequencies below 2 GHz, the output of AR1-C drives amplifier AR3-C and transistor Q4. This provides the current drive for the low frequency PIN leveler in switch S7 (located on RF Deck Assembly). Potentiometer R86 adjusts the offset for the frequncy range. When operating at output frequencies above 2 GHz, an active low signal at pin 18 of the board closes analog switch D14-S14 which turns the low band leveler fully on (no attenuation).

3-29. The circuit consisting of comparator AR2-C, transistor Q5, and associated components is the driver for the UNLEVELED indicator located on the front panel. If the output of AR1-B exceeds the voltage level established by zener diode VR1, the output of AR2-C goes low turning on the UNLEVELED indicator. Transistor Q5 conducts when a high level signal is present on pin 23 of the board. This forces the output of AR2-C high which turns off the UNLEVELED indicator. The microprocessor controls this input when the unit is not in the closed loop mode (e.g. during modulation or external power measurement).

3-30. Operational amplifier AR1-A is the driver for the front panel power meter LED display. Analog switch D19-S19 is normally closed providing an input for the power meter voltage. An offset voltage of +1 Vdc is applied through contacts 2 and 3 of analog switch U5 and voltage divider R41 and R42 to compensate for the 10 dB couplers in series with the power meter input. The WJ-1204 has a manual power meter calibration function. Pressing the front panel CAL button causes pin 8 of U5 to go low and pin 9 of U5 to go high. The low on pin 8 opens switch D19-S19 removing the power meter correction voltage from the display driver. Contacts 10 and 11 of U5 are closed which grounds the summing junction of AR1-A so that the display will read zero. Releasing the CAL button returns these switches to their normal positions. The CAL button also causes the microprocessor to force pin 32 of

the board high which triggers the sample and hold circuit.

3-31. The circuitry consisting of quad comparator AR5, quad AND gate U16, analog switch U17 and U18-B, and comparator AR2-B is used to prevent the TWTA (AR3 on RF Deck Assembly) from going into an overdrive condition. Effectively, this circuit adds fixed amounts of attenuation into the PIN diode leveler that the leveling loop cannot take out. The purpose is to prevent oversaturation of the tube. At programmed output frequencies below 8 GHz, pin 9 of this board is high (approximately +28 V) causing pin 13 of AR2-B to go low disabling all of the U16 AND gates. The low output of all four AND gates places R28 into the collector circuit of Q2 while open-circuiting both R10 and R11. At the same time, resistor R109 is short-circuited. This is the normal configuration in which the circuit has total control over the amount of attenuation in the levelling loop. At programmed output frequencies above 8 GHz, the TWTA is in the loop and pin 9 of the board goes low (approximately zero volts). This forces pin 13 of AR2-B high and enables all of the U16 AND gates. A sample of the YIG multiplier tuning voltage is fed to the inverting inputs of quad comparators AR5 via pin 17 of the board and four 1 kilohm input resistors. For each Multiplier Assembly, this tuning voltage is directly proportional to the output frequency of the YIG filter. Potentiometers R57 through R60 establish reference voltage levels at the non-inverting inputs of AR5. These voltage levels correspond to the frequencies at which added attenuation is desired in the leveling loop. The outputs of AR5 control the states of the U17 and U18-B analog switches through the respective U16 AND gates. Table 3-5 summarizes the results and figure 3-6 shows the switch positions for the case with all outputs low.

3-32. KEYBOARD AND DISPLAY CCA A1. The Keyboard and Display Assembly contains the circuitry required for entering data into the WJ-1204-1 and displaying the frequency and available power of the output signal. Analog-to-digital converter (A/D) U8 converts a dc voltage (which corresponds to the equivalent RF power) into digital information for display by light-emitting diodes (LED) DS6 through DS9. These LEDs (except DS6) are designed so that digital data strobed into the display (by NAND gates U7) at the A, B, C, and D inputs are also available at the Q_A, Q_B, Q_C, and Q_D outputs. Data selectors U5 and U6 receive this data and then transfer it to the data bus through bidirectional bus driver U9. Keyboard commands, entered through the switch matrix, are also output to the microprocessor through U9. To accomplish this, the keyboard is constantly scanned (addressed) by address bus decoder U2. When a keyboard switch is pressed, a path is established between U2 and U9, thus loading the data bus with the selected information. When the ENT pushbutton is pressed, the new frequency data is processed by the microprocessor and subsequently displayed

Table 3-5. Switching Action of A4U16

A4U16 Outputs				R28	R110	R111	R109	Added attenuation
A	B	C	D					
0	0	0	0	IN	OUT	OUT	OUT	Least
0	0	0	1	OUT	OUT	IN	OUT	
0	0	1	1	OUT	IN	OUT	OUT	
0	1	1	1	OUT	OUT	OUT	OUT	
1	1	1	1	OUT	OUT	OUT	IN	Most

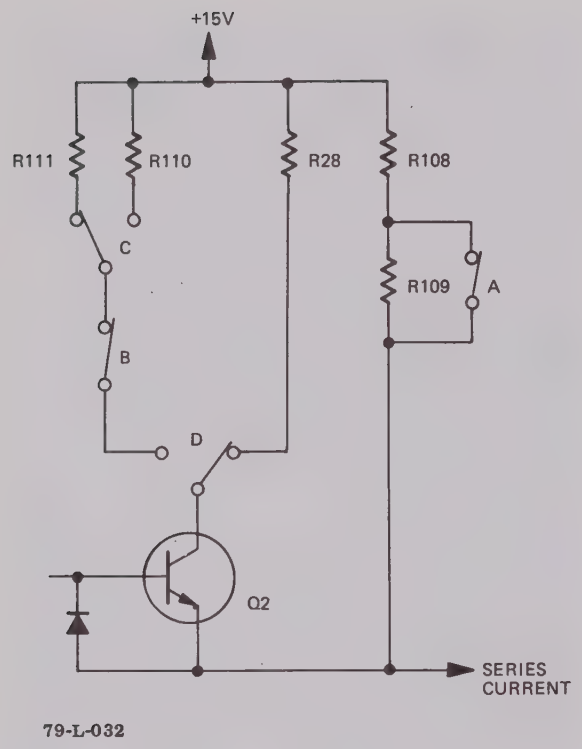


Figure 3-6. Switch Positions For Low U16 Outputs

by LEDs DS1 through DS5. These LEDs are sequentially addressed by U1 and simultaneously supplied with digital frequency data by U9. The data is latched into the display and needs no refresh. The display will remain unchanged until a new frequency is entered at the keyboard. Oscillator U3 is held in a reset state and its Q output (pin 3) is a logic 0. This condition leaves the blanking input to the LEDs (pin 11) inactive. However, when an illegal frequency is entered into the unit, the reset is removed from U3, thus allowing it to oscillate and reciprocally blank and unblank the display (indicating that an illegal entry has been made). Pressing the CLR key on the keyboard resets U3 and returns the LED display to the last valid frequency entered.

3-33. POWER DISTRIBUTION. Primary ac power is supplied to the WJ-1204-1 through an ac input filter module (figure 5-8). This module suppresses any noise that may be present on the line voltage. The front panel POWER switch controls the application of ac power to the power supply and to the traveling-wave tube amplifier (TWTA), AR3. Power supply PS1 is a regulated, current limited, and overvoltage protected power supply that supplies the WJ-1204-1 with all operating dc voltages. The dc voltages supplied by PS1 are output to the Motherboard and from there are distributed to the rest of the unit as shown in figure 5-9.

3-34. UNDERSTANDING INTEGRATED CIRCUITS. The WJ-1204-1 incorporates the latest digital and linear state-of-the-art ICs. A thorough understanding of these ICs is essential if one is to do any maintenance work on the equipment. The following paragraphs present an overview of IC principles as they apply to the WJ-1204-1. The information contained in these paragraphs is intended as a quick reference for maintenance personnel and is not meant to be all-inclusive.

3-35. BASIC INTEGRATED CIRCUIT TYPES. There are two basic types of integrated circuits: digital and linear. Digital ICs are the integrated circuit equivalents of basic transistor logic circuits. A digital IC is a complete functioning logic network, usually requiring nothing more than an input, output, and power source. They are generally repetitive and concerned with only two levels of voltage or current. Linear ICs are the integrated circuit equivalents of basic transistor circuits. Although linear ICs are complete functioning circuits, they often require additional external components for satisfactory operation. Typical examples are: a resistor to convert a linear amplifier into an operational amplifier, a resistor-capacitor combination to provide frequency compensation, and an inductor-capacitor combination to form a filter. Figure 3-7 shows several examples of digital and linear integrated circuits. Another kind of IC is neither digital nor linear, but a

combination of both. Two examples are digital-to-analog converters and analog-to-digital converters.

3-36. DIGITAL INTEGRATED CIRCUITS.

3-37. Logic Families. There are certain operating characteristics among digital ICs that make them unique and not compatible with other digital ICs. This is the basis for classifying digital ICs in logic families. Six

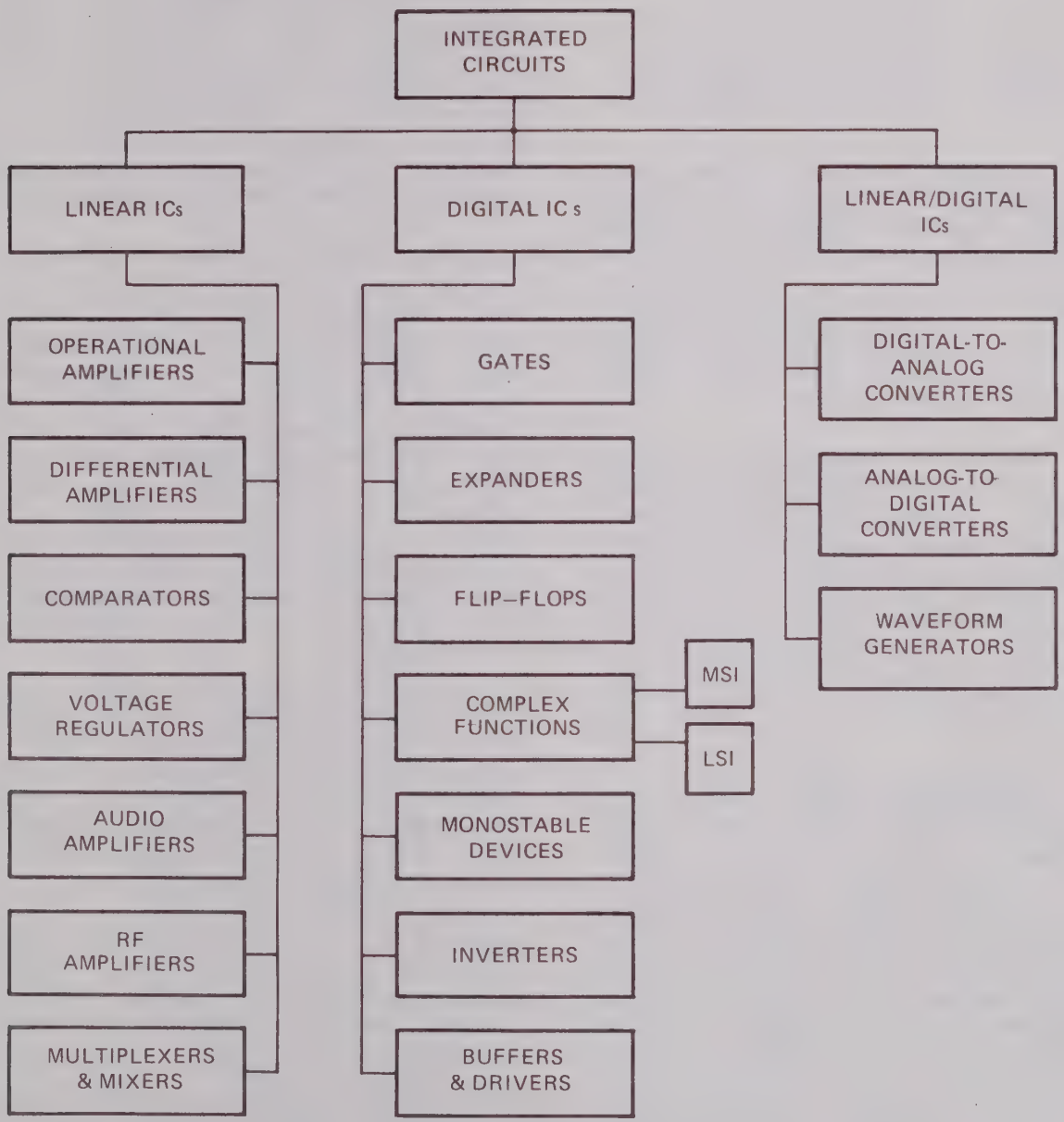


Figure 3-7. Integrated Circuit Types

of the largest and best known logic families currently in use are:

TTL-	transistor-transistor logic
ECL-	emitter-coupled logic (also referred to as current-mode logic)
CMOS-	complementary metal oxide semiconductor logic
DTL-	diode-transistor logic
RTL-	resistor-transistor logic
HTL-	high-threshold logic

3-38. In addition, there are a large variety of logic circuits made by MOS technology. However, the MOS technology (except for CMOS) is used almost entirely for the production of specialized large scale integration (LSI) circuits, such as memories, microprocessors, and custom circuits. Therefore, MOS is usually not defined as a logic family, but as individual LSI products.

3-39. Table 3-6 summarizes the operating characteristics and features of the six logic families. All devices within a logic family are compatible with each other. However, performance specifications sometimes require that two logic families be used in the same circuit. When this is necessary, level translators are used to interface the two logic families. In the WJ-1204-1, only three of the six families are used: TTL, MOS, and ECL.

3-40. Combinational Logic. Most digital equipment consists of two general kinds of logic circuits: combinational and sequential. In a combinational logic circuit, the output depends on the input combination present when the output is examined. But a sequential logic circuit contains memory elements, so that the output depends not only on the state of the input at any given instant but also on the entire input history of the circuit. For this reason, combinational logic elements are sometimes referred to as decision making elements. There are three basic elements: the AND gate, the OR gate, and the Inverter (see figure 3-8). As previously stated, the output from each of these gates depends on the input combination. By studying and memorizing the truth tables for each of the gates shown in figure 3-9, you can understand almost any digital system, no matter how complex. The operation of these gates can also be expressed in Boolean algebra. The AND operation is indicated by the multiplication sign (•), the OR operation is indicated by the addition sign (+), and the NOT (or inversion) operation is indicated by a bar over a symbol. The sign used for an Exclusive OR gate is an addition sign within a circle (⊕). The Boolean expression for each logical operation is also shown in figure 3-9.

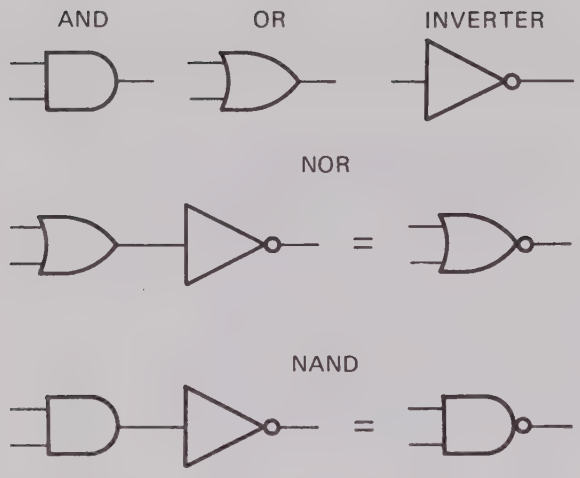
3-41. Data sheets and most truth tables, or function tables, use the HIGH and LOW notation instead of the Logic 1 and 0 states. This is because many systems define the logic 1 state as the most positive voltage equivalent and the logic 0 as the most negative, whereas other systems define logic 1 as the most negative voltage and logic 0 as the most positive. The former is referred to as Positive Logic System and the latter as Negative Logic System. In order to avoid confusion over which notation is being used, it is now standard practice to use the HIGH and LOW states instead of the 1 and 0 states.

3-42. Sequential Logic. Just as there are basic elements in combinational logic circuits, there are basic elements in sequential logic circuits. These elements are sometimes referred to as memory elements because of their ability to store binary information. All memory elements are based upon the reset-set (RS) latch or flip-flop (figure 3-10). This circuit is very important because it is the starting point for understanding more complex flip-flops. Once you become thoroughly familiar with the RS flip-flops, you will find other flip-flops much easier to analyze and use. An important aspect of sequential logic is that it has an added dimension of time. The majority of flip-flop memory elements have a

Table 3-6. Major Logic Families

Parameters	Standard TTL	ECL	CMOS	DTL	RTL	HTL
Supply voltage	5.0V ± 10%	-5.2V ± 10%	3-18 V	5.0V ± 10%	3.0V ± 10%	15 ± 1V
Typical fanout	10	10-25	50 or higher	8	5	10
Propagation delay	10 ns	1-4 ns	20-70 ns	30 ns	12 ns	150 ns
Typical power dissipation per gate	12 mW	22-60 mW plus load	0.01 mW static ≈1 mW at 1 MHz	8-12 mW	12 mW	55 mW
Typical clock rate for flip-flops	35 MHz	70-400 MHz	5 MHz	12-30 MHz	8 MHz	4 MHz
Logic 1 (High) (Typical)	≥2V	-0.75V	≥2V*	≥4.5V	≥1.0V	≥8.5V
Logic 0 (LOW) (Typical)	≤0.8V	-1.2 to -1.8V	≤0.8V*	≤2V	≤0.3V	≤6.5V

*Threshold voltages for CMOS vary according to supply voltage used.



78-L-008

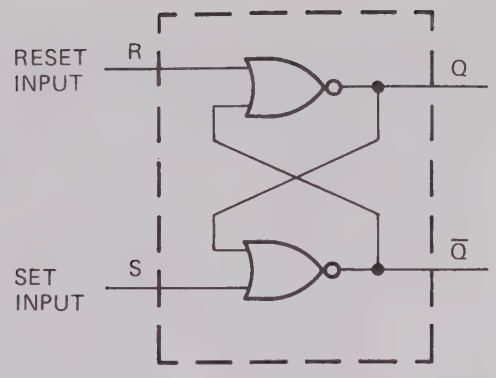
Figure 3-8. Basic Combinational Logic Elements

LOGIC SYMBOLS	TRUTH TABLES		
	INPUT A	INPUT B	OUTPUT C
OR			
$\bar{A} \cdot \bar{B} = \bar{C}$; $A+B = C$	0	0	0
	0	1	1
	1	0	1
	1	1	1
AND			
$A \cdot B = C$; $\bar{A}+\bar{B} = \bar{C}$	0	0	0
	0	1	0
	1	0	0
	1	1	1
NAND			
$A \cdot B = \bar{C}$; $\bar{A}+\bar{B} = C$	0	0	1
	0	1	1
	1	0	1
	1	1	0
NOR			
$\bar{A} \cdot \bar{B} = C$; $A+B = \bar{C}$	0	0	1
	0	1	0
	1	0	0
	1	1	0
EXCLUSIVE OR			
$A+B = C$	0	0	0
	0	1	1
	1	0	1
	1	1	0

NOTE: *On all TTL gates any unconnected input is interpreted as a logic 1. (An unconnected input is referred to as a* floating input.*)*

78-L-010

Figure 3-9. Reference Chart For Decision Making Elements



78-L-011

Figure 3-10. Basic RS Latch

clock input, and their states change only after a transistion of the clock. There are six kinds of flip-flops (FF):

RS FF
Clocked RS FF
T FF (toggle flip-flop)
D FF (delay flip-flop)
J-K FF
Clocked J-K FF

3-43. Table 3-7 summarizes the operation each FF and Figure 3-11 illustrates the basic FFs.

3-44. LINEAR INTEGRATED CIRCUITS. The most common form of linear IC is the operational amplifier (op amp). Operational amplifiers are high-gain, direct-coupled circuits where the gain and frequency response are controlled by external feedback networks. With the use of external feedback networks, the op amp can produce a broad range of intricate transfer functions making it adaptable to many widely differing applications. For example, the same op amp, with a modified feedback network, may be used to form a differential dc amplifier, bridge amplifier, analog integrator, differentiator, line-driving amplifier, current-to-voltage converter, reference voltage source, voltage regulator, current amplifier, or an active filter. The details of these

Table 3-7. Master FF Truth Table

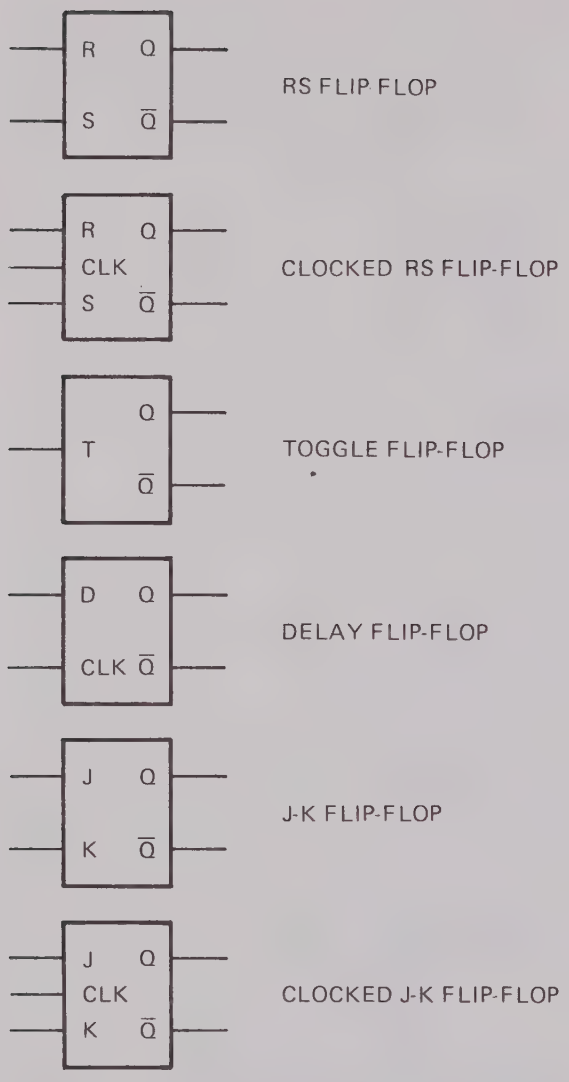
Inputs							Outputs					
							R-S	Clocked R-S	T	D	J-K	Clocked J-K
S	R	T	D	J	K	CLK	Q_{n+1}	Q_{n+1}	Q_{n+1}	Q_{n+1}	Q_{n+1}	Q_{n+1}
0	0						Q_n					
0	1						0					
1	0						1					
1	1						*					
0	0					0		Q_n				
0	0					1		Q_n				
0	1					0		0				
0	1					1		1				
1	0					0		Q_n				
1	0					1		$\overline{Q}_n$				
1	1					0		Q_n				
1	1					1		*				
		0							Q_n			
		1							$\overline{Q}_n$			
			0							0		
			1							1		
				0	0						Q_n	
				0	1						0	
				1	0						1	
				1	1						$\overline{Q}_n$	
				0	0	0						Q_n
				0	0	1						Q_n
				0	1	0						0
				0	1	1						1
				1	0	0						Q_n
				1	0	1						$\overline{Q}_n$
				1	1	0						
				1	1	1						

*Indeterminate

Note:

Q_n = the level of Q before the steady state conditions indicated in the INPUT column have been established.

Q_{n+1} = the level of Q after the steady-state conditions at the INPUT column have been established.

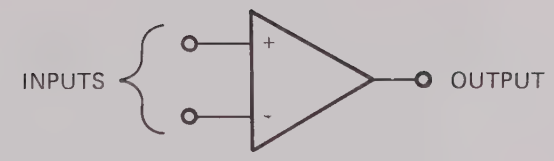


78-L-014

Figure 3-11. Logic Symbols For Flip-Flops

applications are beyond the scope of this manual, as most of these are not used in the WJ-1204-1. However, the basic characteristics of the op amp will be summarized and examples of actual circuits shown for reference.

3-45. Ideal Op Amp Characteristics. The basic op amp is represented by the symbol in figure 3-12. The input denoted by the negative sign is called the inverting input; the plus sign denotes the non-inverting input. (For simplicity, ground, power supply, and frequency-compensation connections are omitted from the figure.) If an input signal is impressed across the inverting terminal with respect to ground, the output signal is 180° out of phase with respect to the input signal. For a signal applied across the noninverting terminal with respect to ground, the output is in phase with the input. If signals are impressed across both the inverting and noninverting terminals with respect to ground, the output is proportional to the difference of the input signals. The characteristics of the ideal op amp, which many physical op amps approach, are:



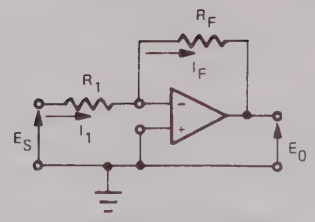
78-L-015

Figure 3-12. Symbol For The Basic Operational Amplifier

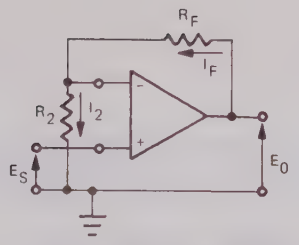
(1) Voltage gain is infinite.
(2) Input impedance is infinite.
(3) Output impedance is zero.
(4) The frequency response is flat (constant) for all frequencies.
(5) The output signal is zero if the input signal is zero.

3-46. Feedback Network. To make the op amp useful and versatile, feedback components are introduced around the amplifier. The most common feedback components are resistors and capacitors. Figure 3-13 shows examples of many of the circuits mentioned. You should realize that there may be several ways of designing any given circuit, but those shown in figure 3-13 are the most common ones that are encountered.

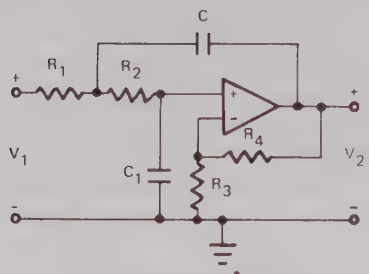
3-47. IC DESCRIPTIONS. All ICs used in the WJ-1204-1 are described in the following paragraphs. Each description includes a logic or block diagram, a function (truth) table, and the pin configuration of the package.



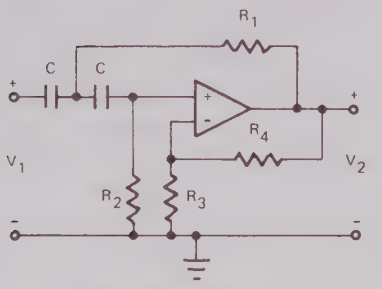
INVERTING AMPLIFIER



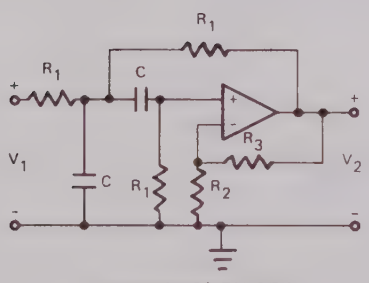
NONINVERTING AMPLIFIER



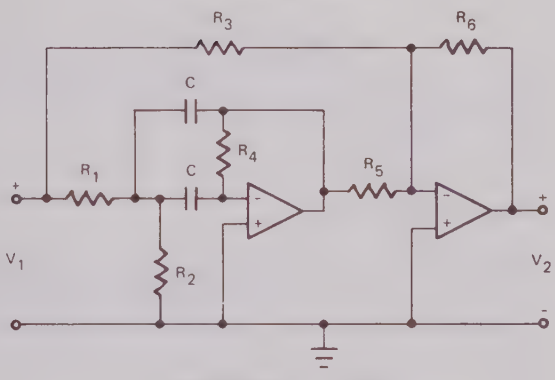
LOW-PASS FILTER



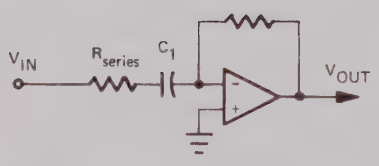
HIGH-PASS FILTER



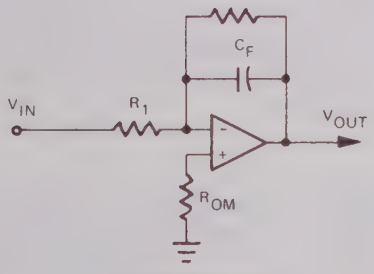
BAND-PASS FILTER



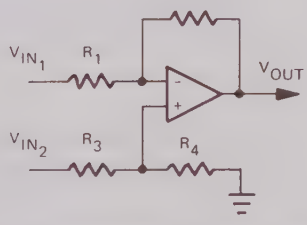
BAND-REJECT FILTER



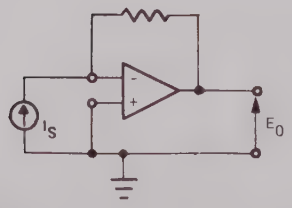
DIFFERENTIATOR



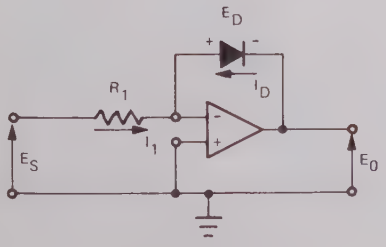
INTEGRATOR



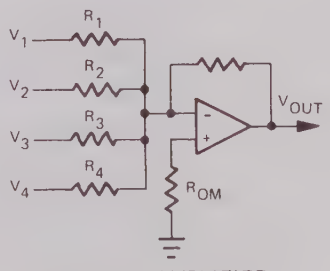
DIFFERENTIAL DC AMPLIFIER



CURRENT-TO-VOLTAGE CONVERTER



LOGARITHMIC AMPLIFIER



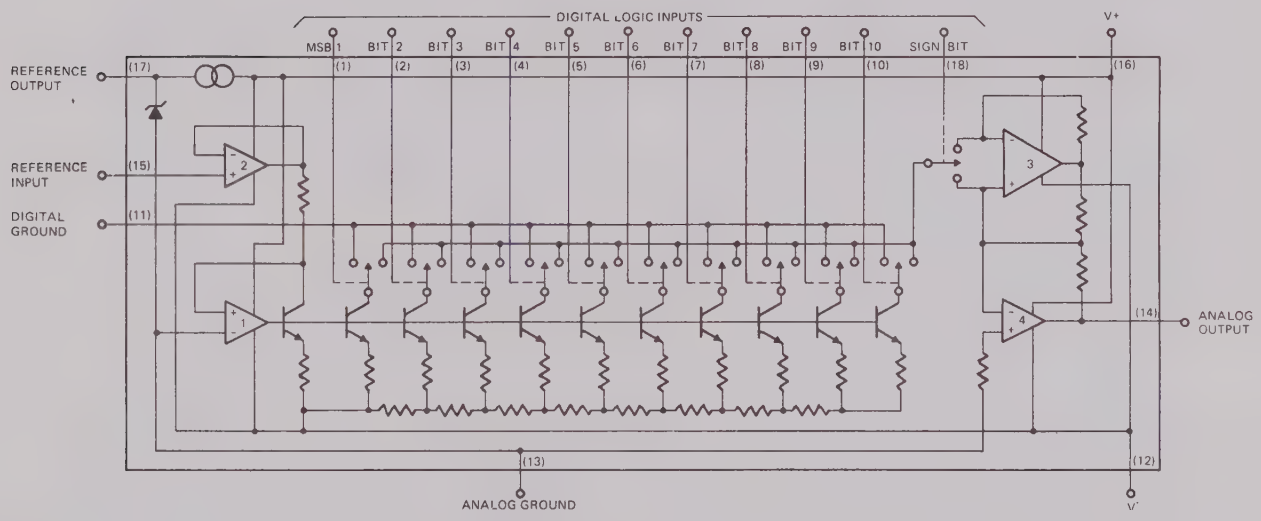
SUMMING AMPLIFIER

78-L-016

Figure 3-13. Basic Op-Amp Applications

3-48. DAC-02 Digital-to-Analog Converter. The DAC-02 (figure 3-14) is a complete 10 bit plus sign D/A converter on a single 82 x 148 mil monolithic chip. All elements of a complete sign/magnitude DAC are included: precision voltage reference, current steering logic, current sources, R-2R resistor network logic, controlled polarity switch, and high speed internally compensated output op amp. Monotonicity guaranteed over the 0 to +70 °C temperature range is achieved by the untrimmed diffused R-2R resistor ladder network. The buffered reference input is capable of tracking over a wide range of voltages.

LOGIC DIAGRAM



POSITIVE SIGN/MAGNITUDE CODING TABLE

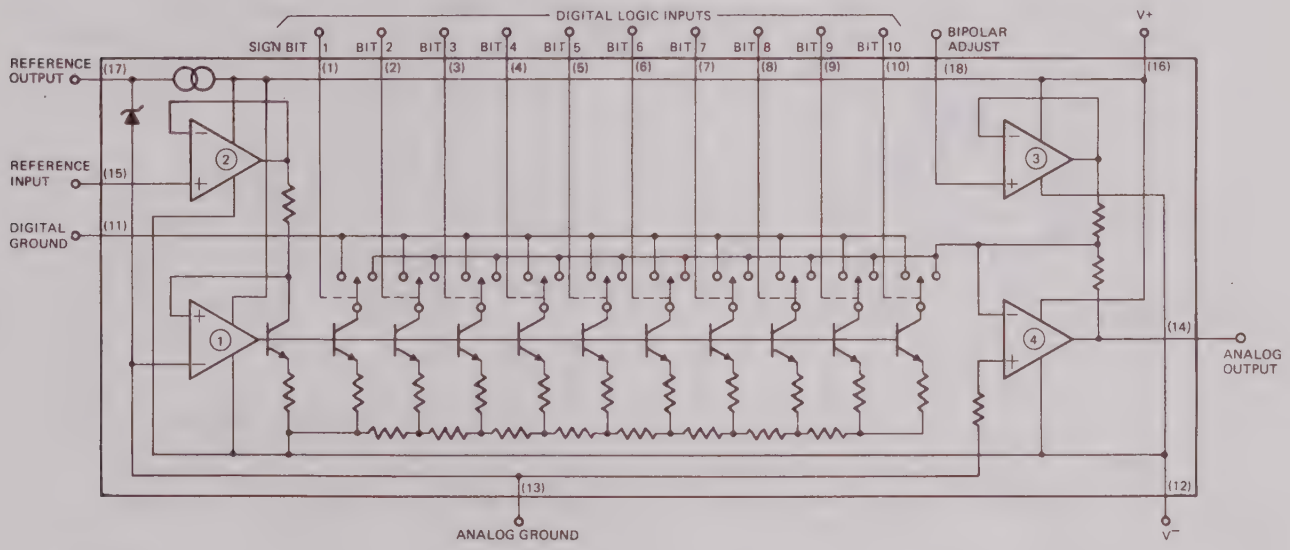
OUTPUT	SIGN BIT	INPUT BITS MSB									LSB
+ FULL SCALE	1	1	1	1	1	1	1	1	1	1	1
+ "HALF" SCALE	1	1	0	0	0	0	0	0	0	0	0
ZERO SCALE (+)	1	0	0	0	0	0	0	0	0	0	0
ZERO SCALE (–)	0	0	0	0	0	0	0	0	0	0	0
– "HALF" SCALE	0	1	0	0	0	0	0	0	0	0	0
– FULL SCALE	0	1	1	1	1	1	1	1	1	1	1

77-L-401

Figure 3-14. DAC-02CCX1 D/A Converter, Simplified Schematic, Pin Configuration and Function Table

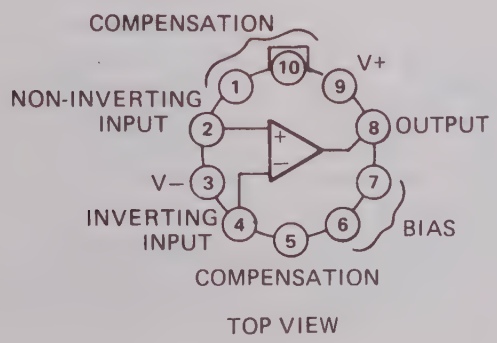
3-49. DAC-04ACX2 Digital-to-Analog Converter. The DAC-04 (figure 3-15) is a complete 10 bit Two's Complement D/A Converter on a single monolithic chip. All elements of a complete bipolar output Two's Complement DAC are included: precision voltage reference, current steering logic, current sources, R-2R resistor network, bipolar offset circuit and high speed internally compensated output op amp. Monotonicity guaranteed over the entire 0 to +70 °C temperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages.

3-50. LH0004 Operational Amplifier. The LH0004 (figure 3-16) is a general purpose operational amplifier designed to operate from supply voltages up to ±40V. The device dissipates extremely low quiescent power, typically 8 mW at 25°C and V_S = ±40V. The LH0004 is specified for operation over the -55°C to +125°C military temperature range. The LH0004C is specified for operation over the 0°C to +85°C temperature range.



79-L-024

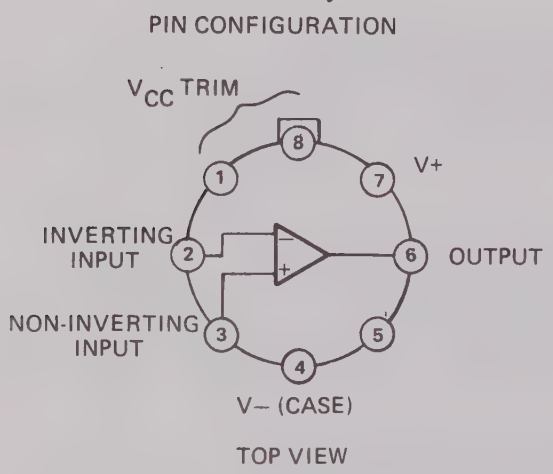
Figure 3-15. DAC-04ACX2 D/A Converter, Simplified Schematic and Pin Configuration Diagram



79-L-020

Figure 3-16. LH0004 Operational Amplifier, Pin Configuration Diagram

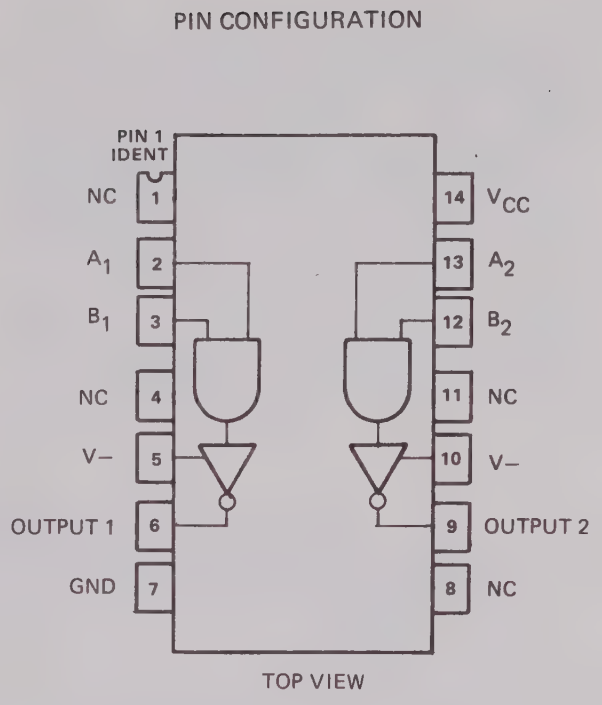
3-51. OP-07 Operational Amplifier. The OP-07 (figure 3-17) is an operational amplifier with a long term stability of 0.2 microvolts per month. Complete elimination of external components for offset nulling, frequency compensation, and device protection permits optimization of system Mean-Time-Between-Failure rates. Low bias currents and extremely high input impedances are maintained over the entire temperature range.



79-L-023

Figure 3-17. OP-07CJ Operational Amplifier, Pin Configuration

3-52. DH0034CD Level Translator. The DH0034CD (figure 3-18) is a high speed dual level translator for interfacing to MOS or junction FET analog switches. It is capable of accepting TTL/DTL input levels and shifting to CML, MOS, or IBM (SLT) logic levels. When both inputs to the DH0034 are raised to logic 1, the output goes low within 15 nanoseconds.



79-L-022

Figure 3-18. DH0034CD Dual Level Translator, Pin Configuration

3-53. DAC-70C Digital-to-Analog Converter. The DAC-70C (figure 3-19) is a 16 bit digital-to-analog converter with internal reference in a 24 pin metal DIP package. It is designed to provide wide dynamic range and preserve accuracy in a compact package. It is specified for -25 to +85° Celcius temperature, ±7 ppm per degree Celsius gain drift, and ±0.003% maximum linearity error. The DAC-70C accepts TTL compatible complementary, 16-bit binary, or 4-digit BCD input codes, and provides current output ranges of ±1 milliamp or 0 to -2 milliamp for driving an external amplifier.

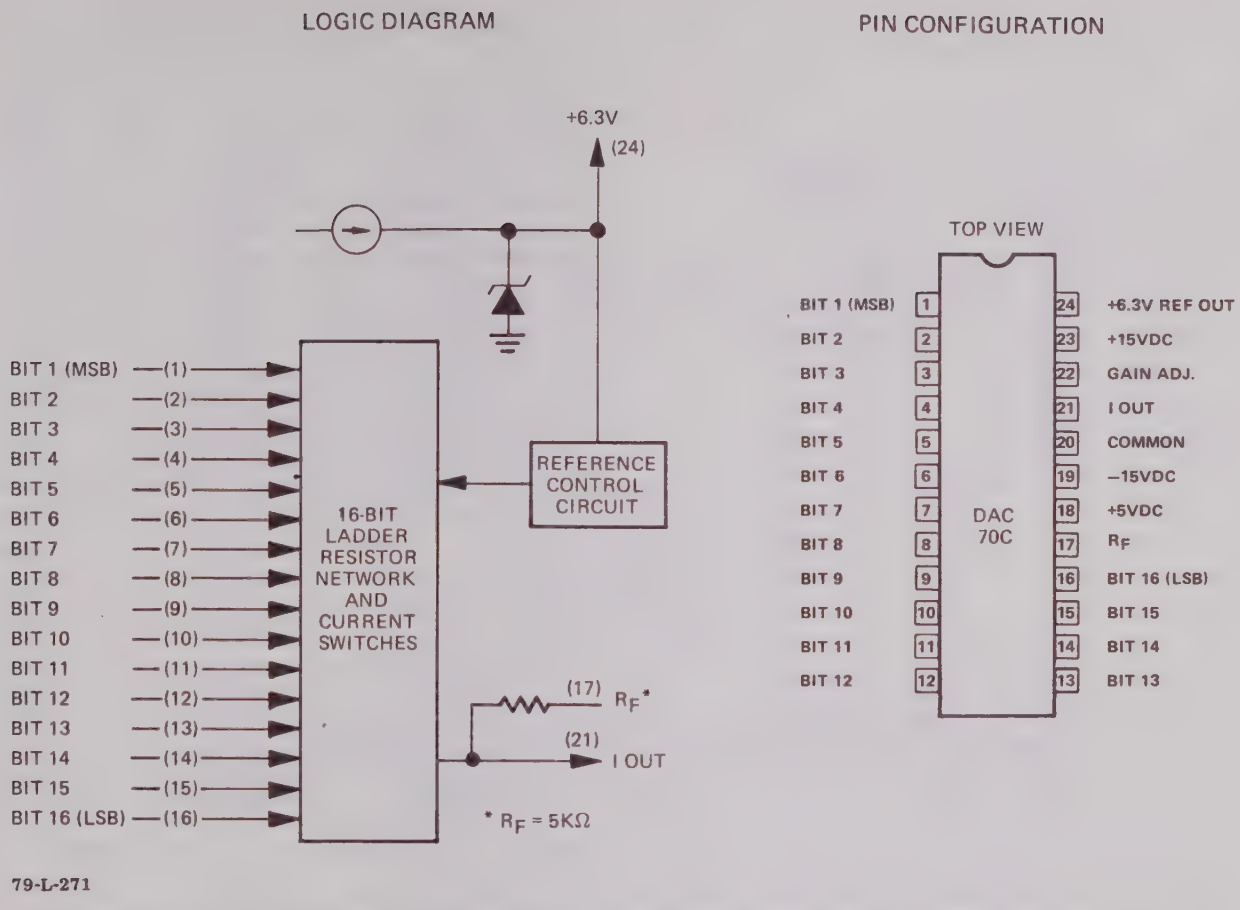


Figure 3-19. DAC-70C D/A Converter, Simplified Schematic and Pin Configuration

3-54. Z-80 CPU Microprocessor. The Z80-CPU (figure 3-20) is a third generation microprocessor. The internal register configuration contains 208 bits of Read/Write memory that are accesible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8 bit registers or as 16 bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. The alternate set allows foreground/background mode of operation or may be reserved for very fast Interrupt response. The CPU also contains a 16 bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting, and simplification of many types of data handling. The two 16 bit index resisters allow tabular data manipulation and easy implementation of relocatable code. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to an interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

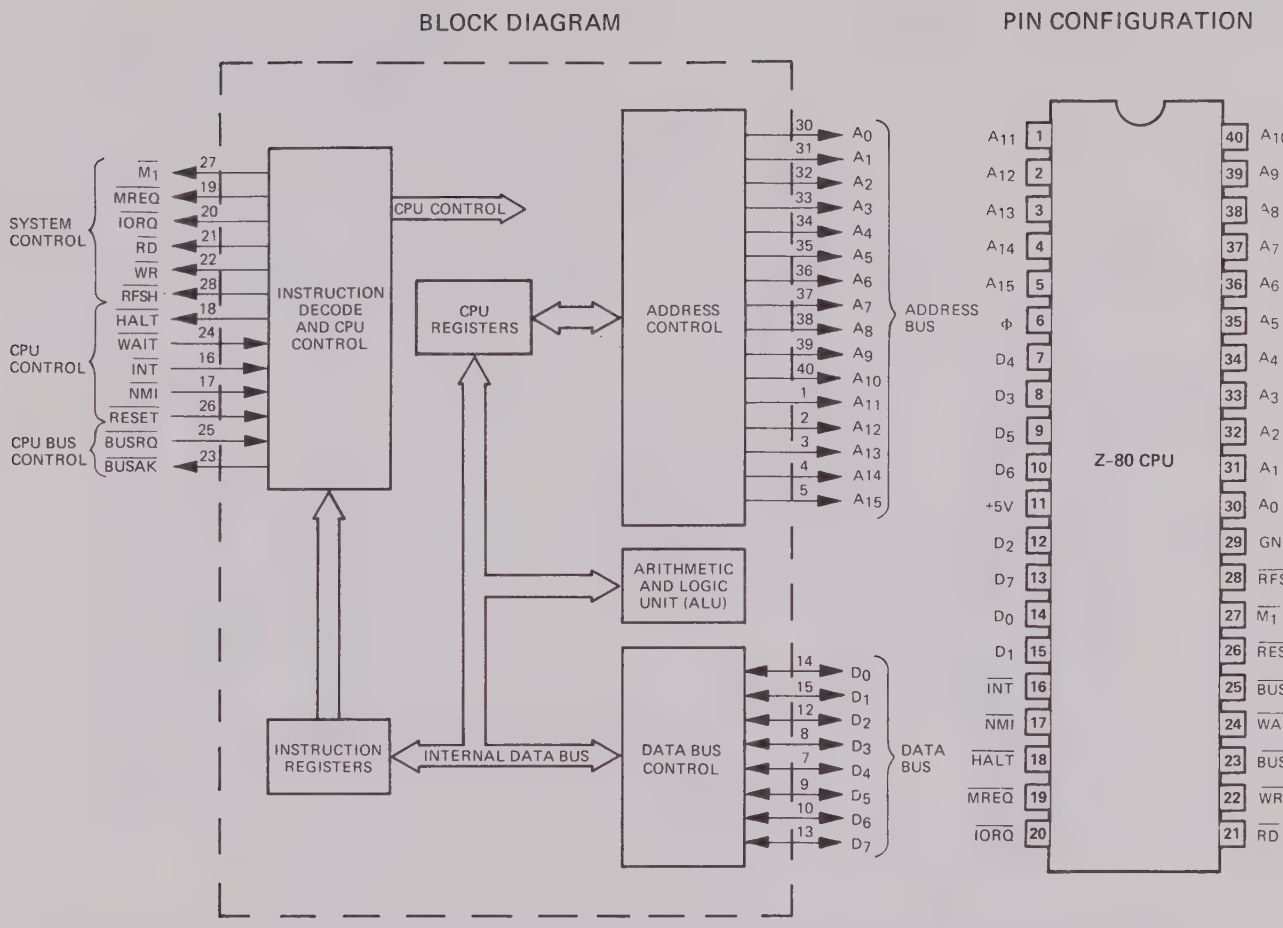


Figure 3-20. Z-80 CPU Microprocessor, Block Diagram and Pin Configuration

3-55. LM101AH Operational Amplifier. The LM101AH (figure 3-21) is a general purpose operational amplifier with overload protection on the input and output. There is no latch-up when the common mode range is exceeded. A single 30 picofarad capacitor keeps it free of oscillations and compensation. Specifications include an offset voltage of 3 millivolts maximum over temperature range; input current of 100 nanoamperes maximum over temperature range; offset current of 20 nanoamperes maximum over temperature range; a slew rate of 10 V per microsecond as a summing amplifier; and differential input voltage of ± 30 V. It is guaranteed over a temperature range of -55 degrees Celsius to +124 degrees Celsius.

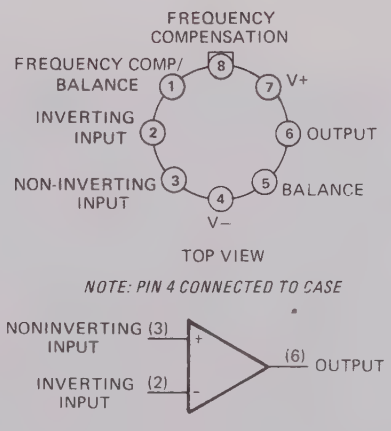
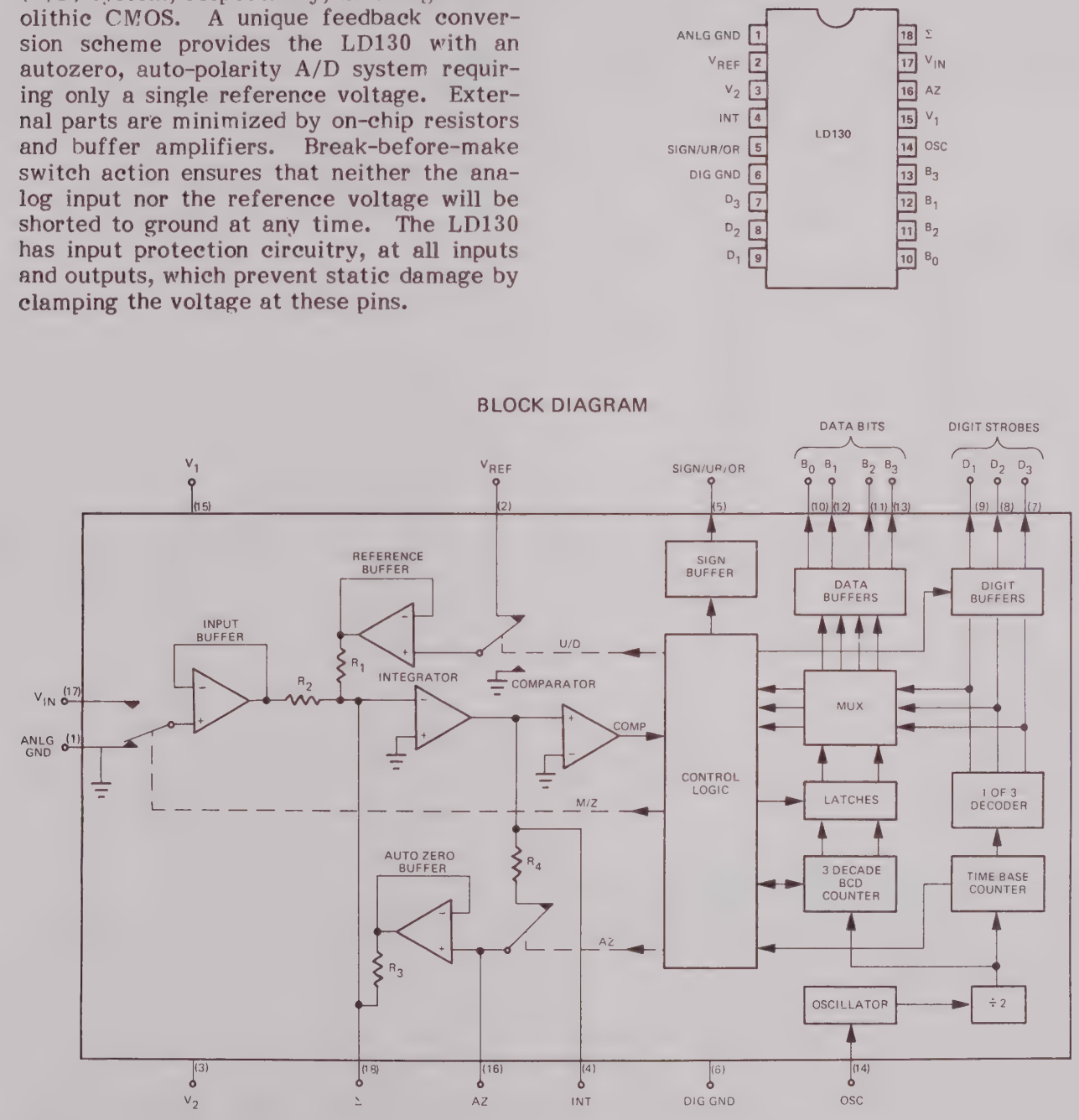


Figure 3-21. LM101AH Operational Amplifie Pin Configuration

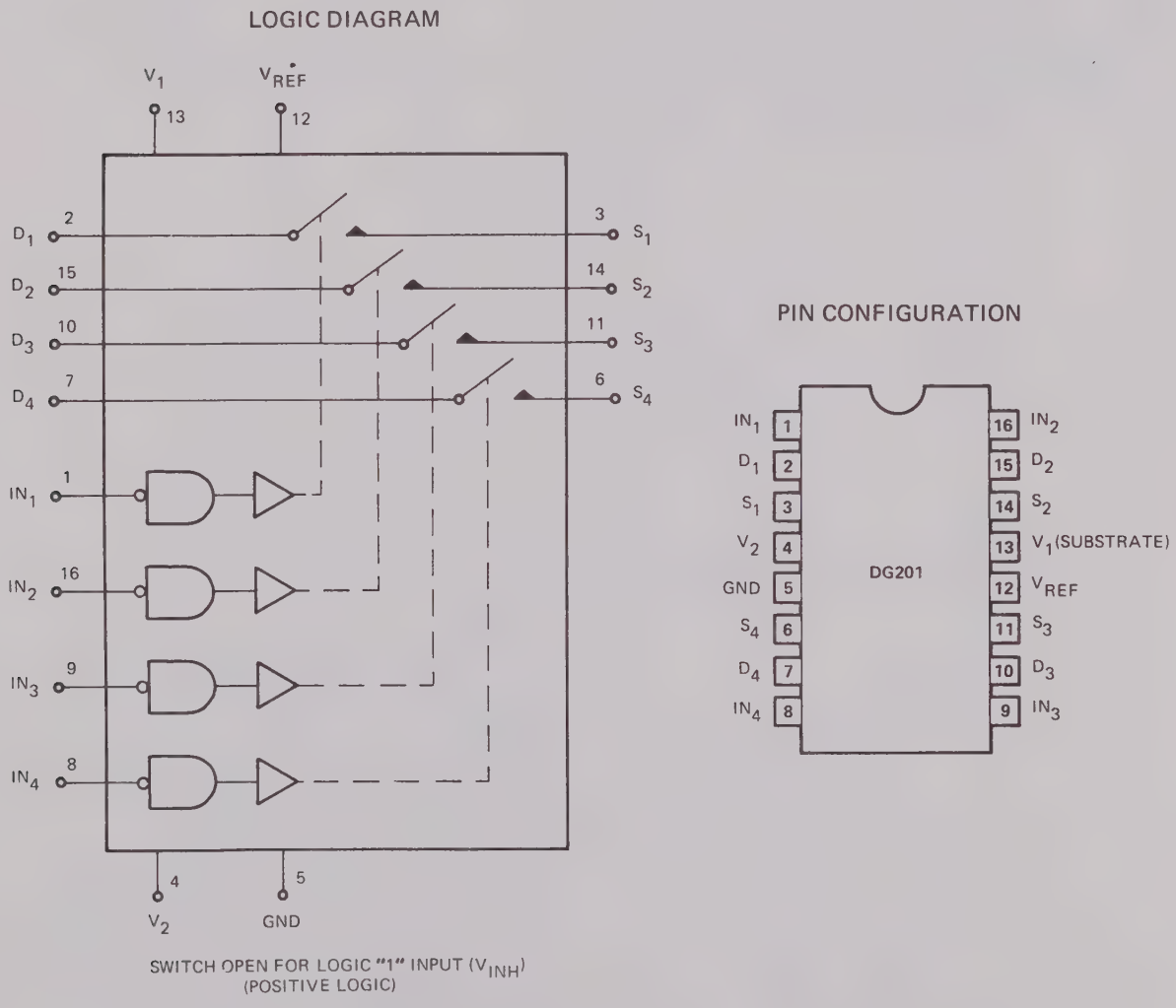
3-56. LD130CJ Analog-to-Digital Converter. The LD130 (figure 3-22) combines both the analog and digital subsystems of a 3 digit and a 3 1/3 digit analog-to-digital (A/D) system, respectively, in a single monolithic CMOS. A unique feedback conversion scheme provides the LD130 with an autozero, auto-polarity A/D system requiring only a single reference voltage. External parts are minimized by on-chip resistors and buffer amplifiers. Break-before-make switch action ensures that neither the analog input nor the reference voltage will be shorted to ground at any time. The LD130 has input protection circuitry, at all inputs and outputs, which prevent static damage by clamping the voltage at these pins.



78-L-007

Figure 3-22. LD130CJ A/D Converter, Block Diagram and Pin Configuration

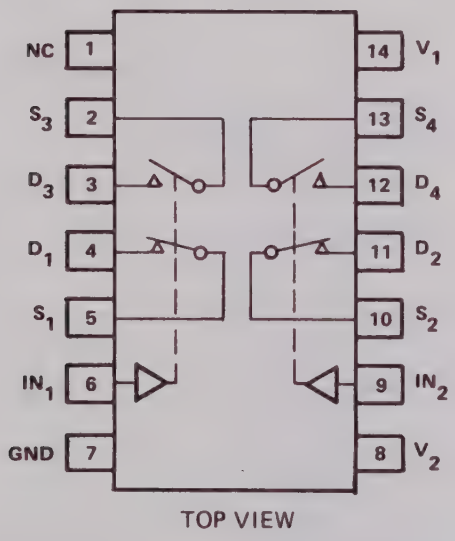
3-57. DG201 Analog Switch. The DG201 (figure 3-23) is a quad single pole, single throw analog switch that uses a parallel combination of a PMOS and a NMOS field effect transistor. In the ON condition, each switch will conduct current in either direction, and in the OFF condition, each switch will block voltages up to 30 V peak-to-peak. The ON-OFF state of each switch is controlled by a driver. With logic 0 at the input, the switch will be ON. With logic 1 at the input, the switch will be OFF. The logic input will recognize voltages between 0 and 0.8 V as logic 0 and voltages between 2.4 and 15 V as logic 1. Switch action is break-before-make.



77-L-405

Figure 3-23. DG201 Analog Switch, Schematic and Pin Configuration

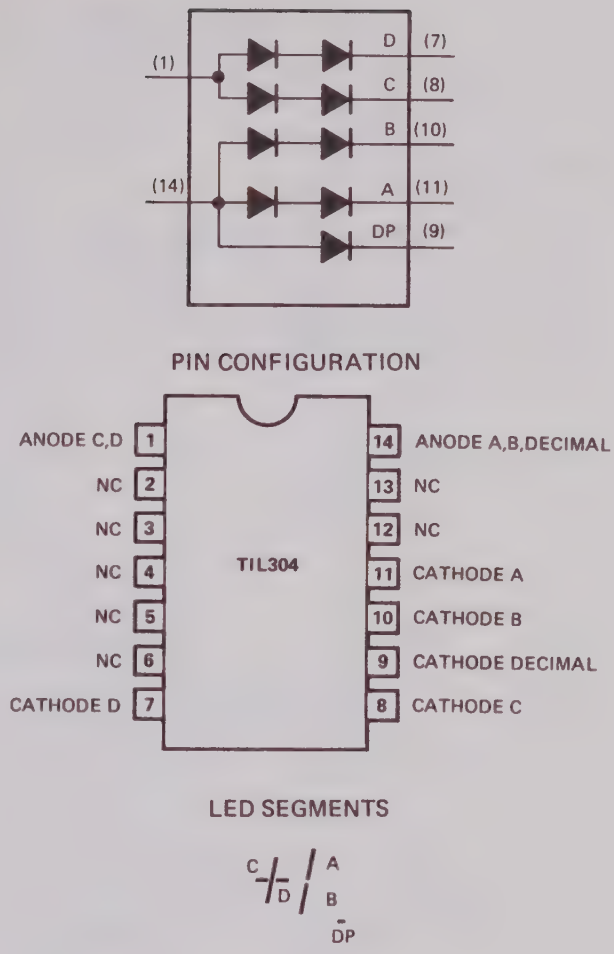
3-58. DG303CJ Analog Switch. The DG303CJ (figure 3-24) is an analog switch that provides a low and nearly constant ON resistance (less than 50 ohms) over the full analog signal. In the ON condition the switches will conduct current in either direction with no offset voltage. In the OFF condition the switches will block voltages up to 30 volts peak-to-peak. A logic input driver controls the ON/OFF state of the switches. The DG303 is TTL input compatible and has a logic 0 state with an input less than 0.8 volts and a logic 1 state with an input greater than 4 volts.



79-L-037

Figure 3-24. DG303CJ Analog Switch, Pin Configuration

3-59. TIL304 Numeric Display. The TIL304 (figure 3-25) is a solid state visible numeric display with red transparent plastic encapsulation.



77-L-439

Figure 3-25. TIL304 Numeric Display, Pin Configuration

3-60. TIL308 Numeric Display With Logic. The TIL308 (figure 3-26) is a solid state visible display chip for use in all systems requiring a display of BCD data. It internally drives a seven segment light-emitting diode (LED) display that contains a five-bit latch and a decoder/LED driver.

Latch Strobe input, Pin 5 - When low, the data in the latches follow the data on the latch inputs. When high, the data in the latches are held constant and are unaffected by new data on the latch inputs.

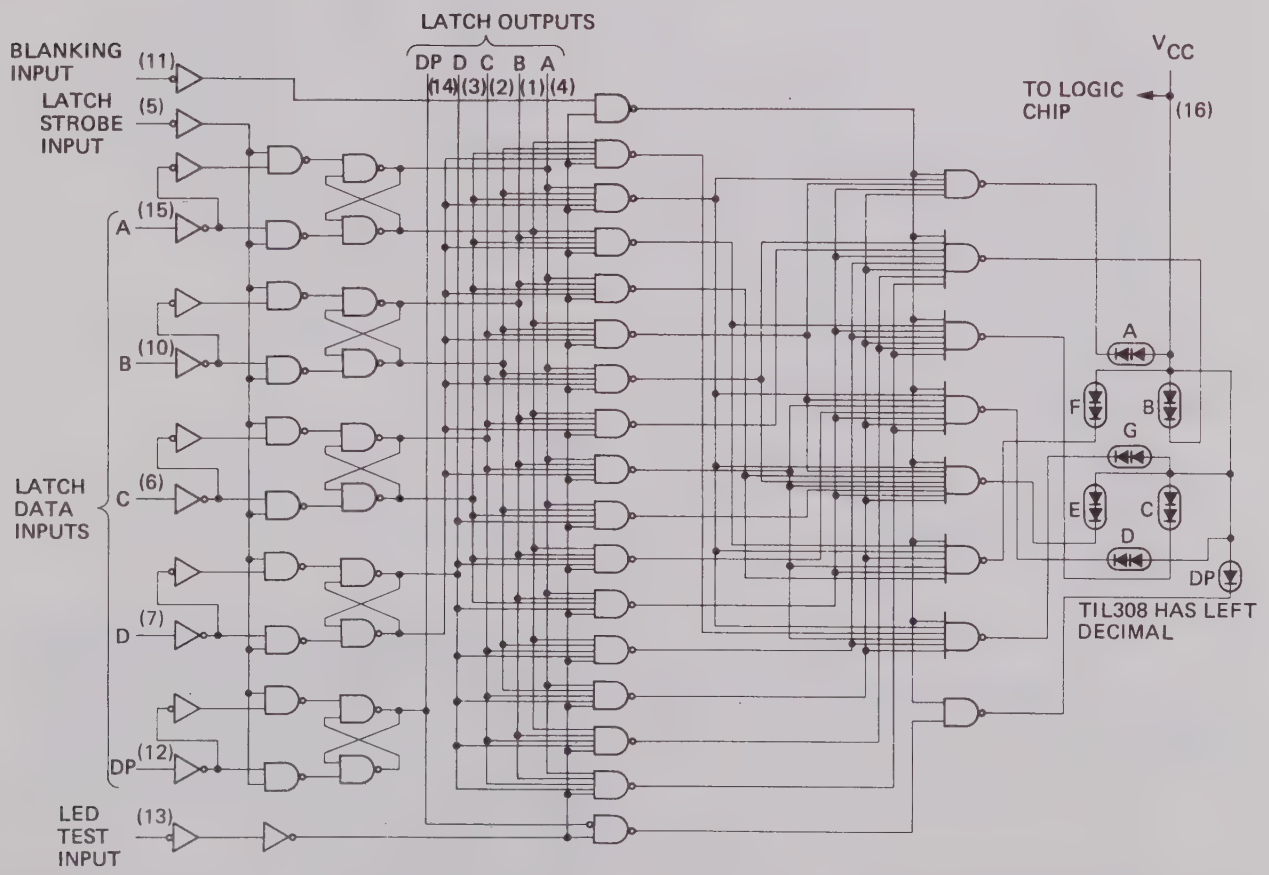
Latch Data inputs, pins 15, 10, 6, 7, and 12 - Data on these inputs are entered into the latches under the control of the latch strobe input. The binary weights of the inputs are: A = 1, B = 2, C = 4, D = 8. DP is decimal point latch data input.

Latch outputs Q_A, Q_B, Q_C, Q_D, Q_{DP}, Pins 4, 1, 2, 3, 14 - The BCD data that drives the decoder is stored in the five latches and is available at these outputs. The binary weights of the outputs are $Q_A = 1$, $Q_B = 2$, $Q_C = 4$, $Q_D = 8$. Q_{DP} is decimal point latch output.

Blanking input, pin 11 - When low, will blank (turn off) the entire display. Must be high for normal operation of the display.

LED Test input, pin 13 - When low, will turn on the entire display, overriding the data in the latches and the blanking input. Must be high for normal operation of the display.

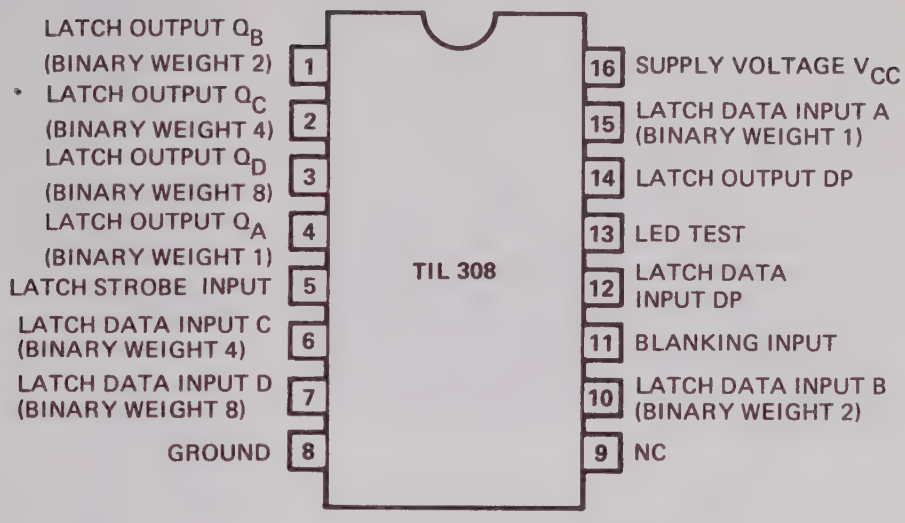
LOGIC DIAGRAM



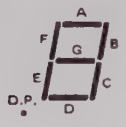
77-L-440/1

Figure 3-26. TIL308 Numeric Display, Schematic and Pin Configuration (sheet 1 of 2)

PIN CONFIGURATION



LED SEGMENTS



FUNCTION TABLE

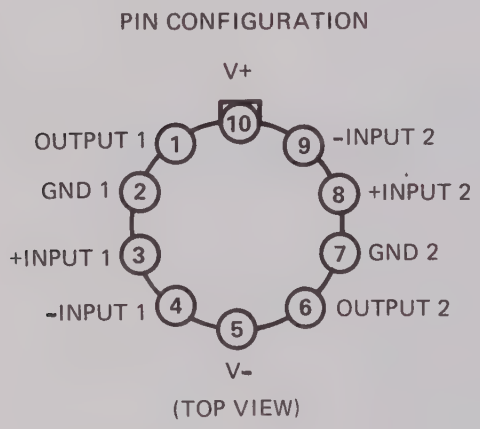
FUNCTION	LATCH INPUTS						BLANKING	LED	LATCH OUTPUTS					DISPLAY
	D	C	B	A	DP	STROBE	INPUT	TEST	Q_D	Q_C	Q_B	Q_A	Q_{DP}	TIL308
0	L	L	L	L	L	L	H	H	L	L	L	L	L	0
1	L	L	L	H	H	L	H	H	L	L	L	H	H	.1
2	L	L	H	L	L	L	H	H	L	L	H	L	L	2
3	L	L	H	H	H	L	H	H	L	L	H	H	H	.3
4	L	H	L	L	L	L	H	H	L	H	L	L	L	4
5	L	H	L	H	H	L	H	H	L	H	L	H	H	.5
6	L	H	H	L	L	L	H	H	L	H	H	L	L	6
7	L	H	H	H	H	L	H	H	L	H	H	H	H	.7
8	H	L	L	L	L	L	H	H	H	L	L	L	L	8
9	H	L	L	H	H	L	H	H	H	L	L	H	H	.9
A	H	L	H	L	L	L	H	H	H	L	H	L	L	A
MINUS SIGN	H	L	H	H	H	L	H	H	H	L	H	H	H	-
C	H	H	L	L	L	L	H	H	H	H	L	L	L	C
BLANK	H	H	L	H	H	L	H	H	H	H	L	H	H	
E	H	H	H	L	L	L	H	H	H	H	H	L	L	E
F	H	H	H	H	H	L	H	H	H	H	H	H	H	F
BLANK	X	X	X	X	X	X	L	H	X	X	X	X	X	
LED TEST	X	X	X	X	X	X	X	L	X	X	X	X	X	.8

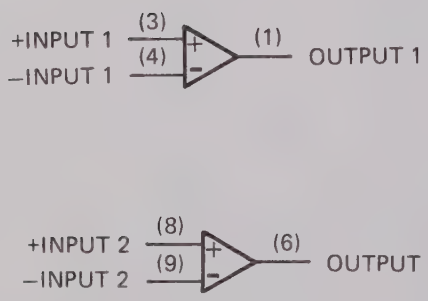
H = high level, L = low level, X = irrelevant.
DP input has arbitrarily been shown activated (high) on every other line of the table.

77-L-440/2

Figure 3-26. TIL308 Numeric Display, Schematic and Pin Configuration (sheet 2 of 2)

3-61. LM319N Dual Comparator. The LM319 (figure 3-27) is a precision high speed dual comparator built on a single monolithic chip. It is designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. The LM319 has two independent comparators, operates from a single 5 V supply, has a typical 80 nanosecond response time at ± 15 V, and minimum fan-out of 2 each side. The maximum input current is 1 microampere over temperature. Inputs and outputs can be isolated from system ground. The LM319 has high common slew rate. It is specified for operation over the zero to +70 degrees Celsius temperature range.

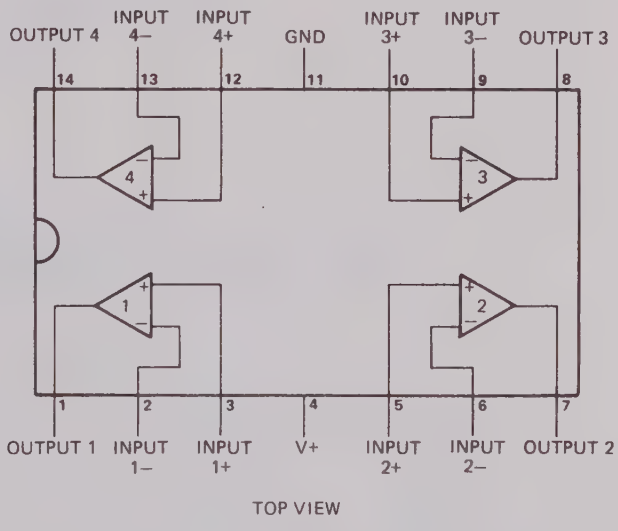




77-L-406

Figure 3-27. LM319N Dual Comparator, Schematic and Pin Configuration

3-62. LM324AN Operational Amplifier. The LM324AN (figure 3-28) is a low power quad op-amp circuit. It consists of four independent, high gain, internally frequency compensated operational amplifiers. In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency and the input bias current are temperature compensated.

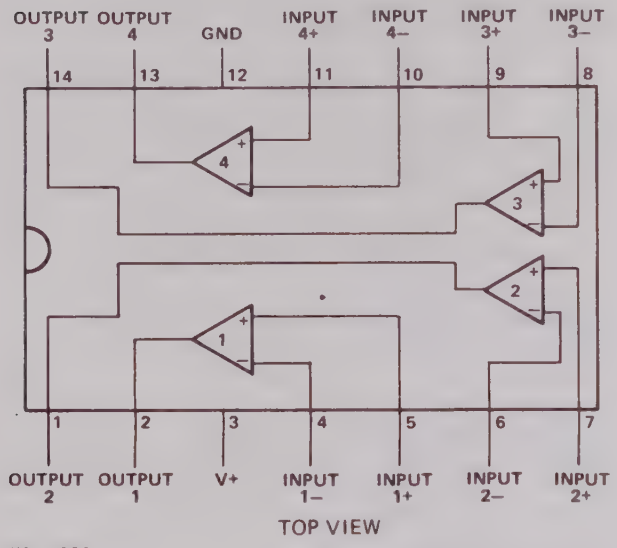


79-L-021

Figure 3-28. LM324AN Quad Operational Amplifier, Pin Configuration

3-63. LM339N Voltage Comparator. The LM339N (figure 3-29) consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode

voltage range includes ground, even though operated from a single power supply voltage.

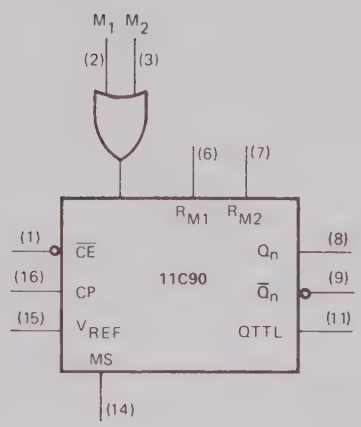


79-L-038

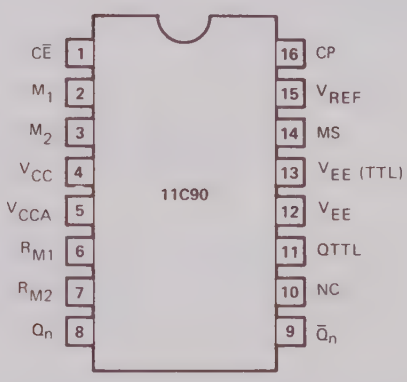
Figure 3-29. LM339N Quad Voltage Comparator, Pin Configuration

3-64. 11C90DC Prescaler. The 11C90DC (figure 3-30) is a high speed ÷10/÷11 prescaler. It will divide by 10 or 11 over a frequency range from dc to typically 650 MHz. The division ratio is controlled by the mode (M) control. The 11C90 contains four ECL flip-flops, an ECL to TTL converter and a Schottky TTL output buffer with an active pull-up. Three of the flip-flops operate as a synchronous shift counter driving the fourth flip-flop operating as an asynchronous toggle. The internal feedback logic is such that the TTL output and the Q4 ECL output are HIGH for six clock periods and LOW for five clock periods. The Mode Control (M) inputs can modify the feedback to make the output HIGH for five clock periods and LOW for five clock periods, as indicated in the Count Sequence Table.

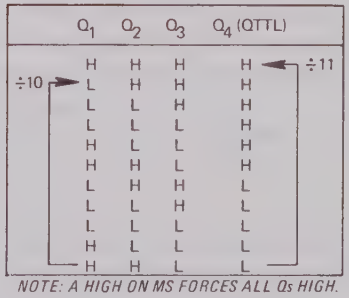
LOGIC DIAGRAM



PIN CONFIGURATION



COUNT SEQUENCE



77-L-407/1

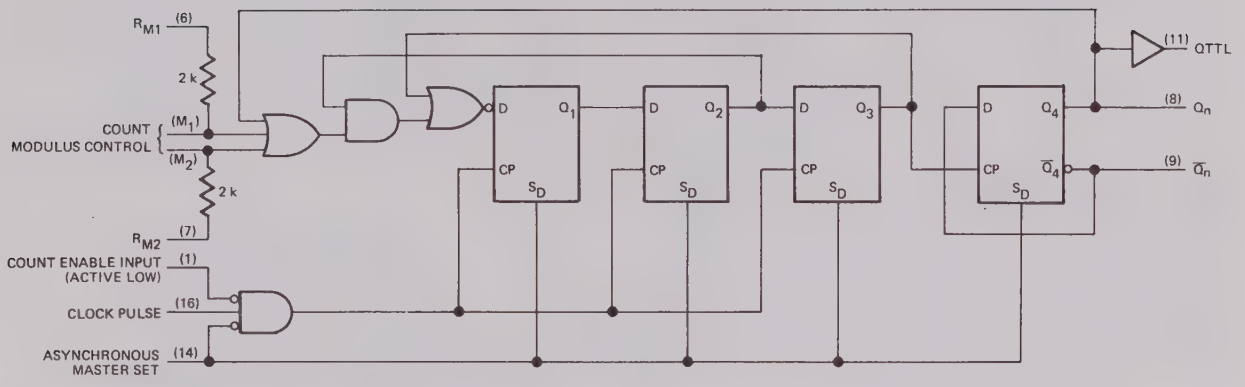
Figure 3-30. 11C90DC ÷10/÷11 Prescaler, Function Diagram and Pin Configuration (Sheet 1 of 2)

OPERATING MODE

INPUTS				OUTPUT
MS	CE	M_1	M_2	RESPONSE
H	X	X	X	SET HIGH
L	H	X	X	HOLD
L	L	L	L	÷11
L	L	H	X	÷10
L	L	X	H	÷10

X = DON'T CARE

BLOCK DIAGRAM



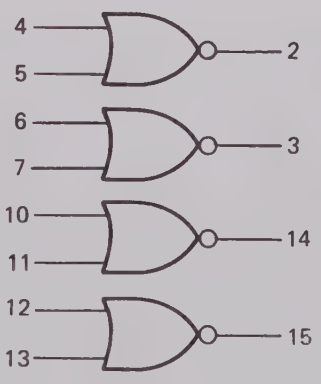
NOTE: THIS DIAGRAM IS PROVIDED FOR UNDERSTANDING OF LOGIC OPERATION ONLY. IT SHOULD NOT BE USED FOR EVALUATION OF PROPAGATION DELAYS AS MANY INTERNAL FUNCTIONS ARE ACHIEVED MORE EFFICIENTLY THAN SHOWN.

77-L-407/2

Figure 3-30. 1190DC ÷10/ ÷11 Prescaler, Function Diagram and Pin Configuration (Sheet 2 of 2)

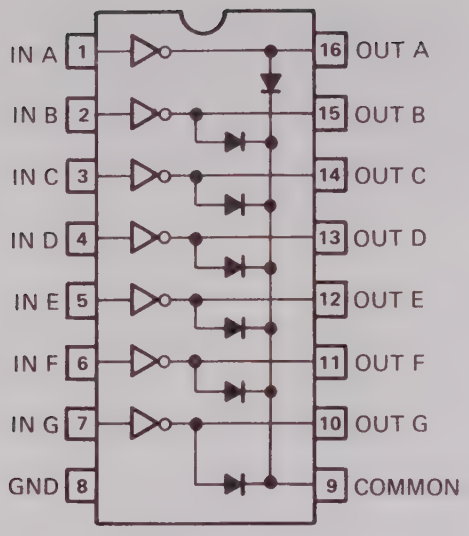
3-65. MC1662L Quad Two-Input NOR Gate. The MC1662L (figure 3-31) provides four 2-input NOR or NAND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range (-30 to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

3-66. ULN2001A Transistor Array. The ULN2001A (figure 3-32) consists of seven NPN transistors in a Darlington-pair configuration. It provides an inverted signal at the output, essentially providing a NAND function. The ULN2001A is used in applications requiring high current and high voltage outputs for driving lamps, relays, etc.



79-L-017

Figure 3-31. MC1662L Quad NOR Gate, Schematic and Pin Configuration

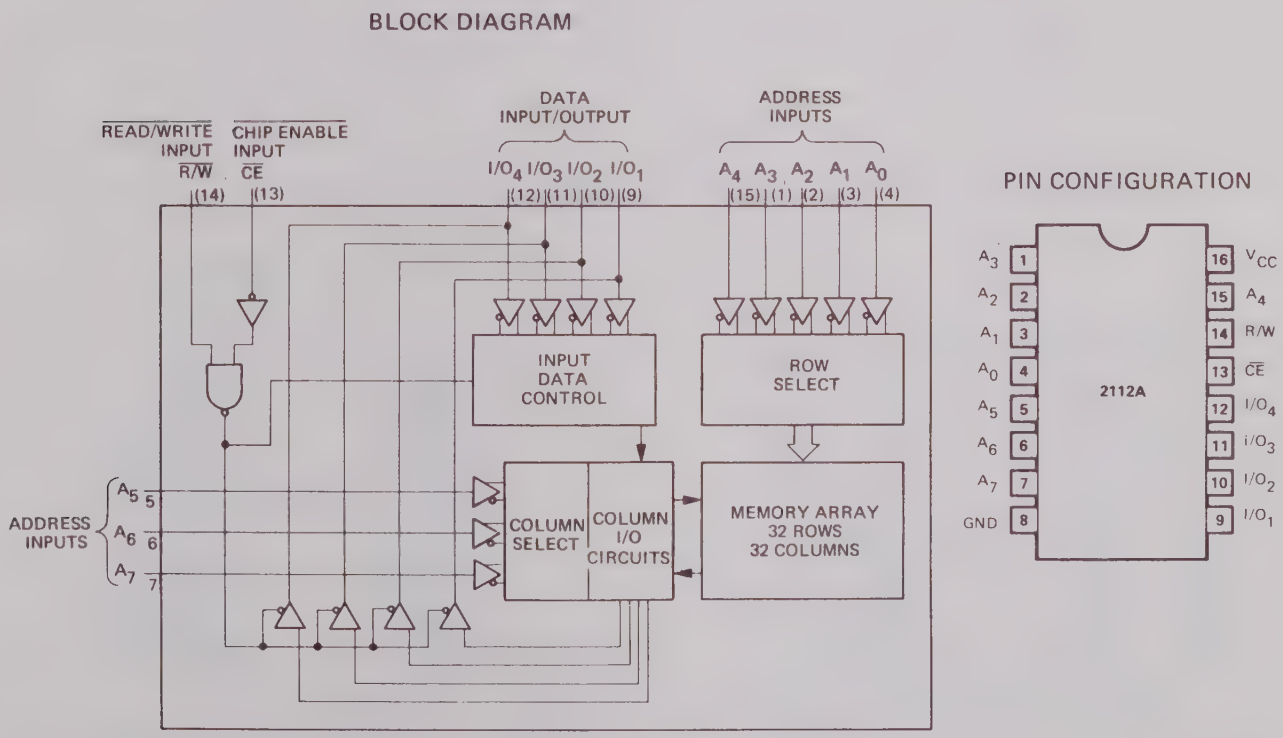


79-L-019

Figure 3-32. ULN2001A Transistor Array, Pin Configuration

3-67. 2112A-4A Random Access Memory. The 2112-4A (figure 3-33) is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided. It is directly TTL compatible in all respects: inputs, outputs, and a single +5 V supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

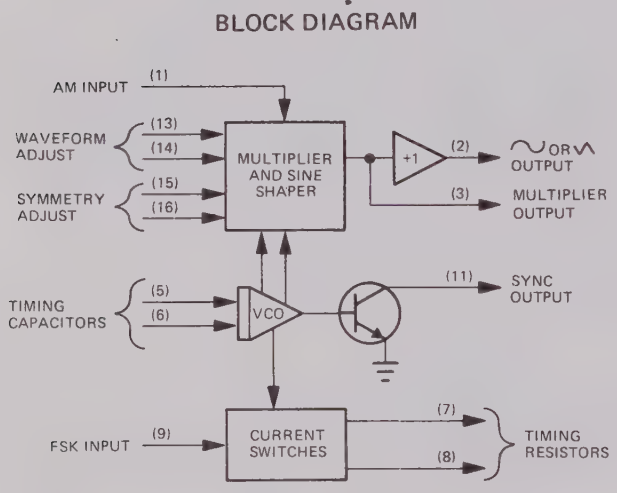
3-68. XR2206 Function Generator. The XR2206 (figure 3-34) is a monolithic function generator integrated circuit capable of producing sine, square, triangle, ramp, and pulse waveforms. The output waveforms

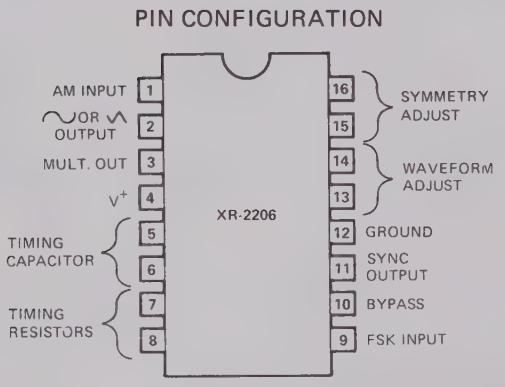


77-L-411

Figure 3-33. 2112A-4A Random Access Memory, Block Diagram and Pin Configuration

can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz. The circuit is comprised of four functional blocks: a voltage-controlled oscillator (VCO); an analog mulitplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches. For sinewave output, amplitude is approximately 60 millivolts peak per kilohm of R3; for triangle, the peak amplitude is approximately 160 millivolts peak per kilohm of R3.

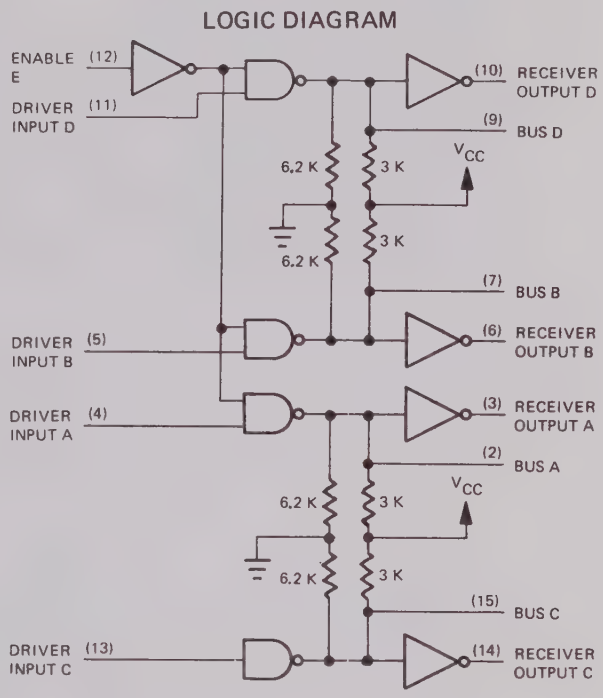


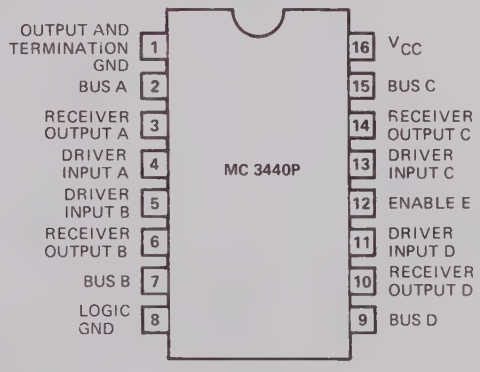


78-L-017

Figure 3-34. XR-2206 Function Generator, Block Diagram and Pin Configuration

3-69. MC3440P Interface Transceiver. The MC3440P (figure 3-35) is a quad interface transceiver designed to meet the general purpose interface bus specification of IEEE Standard 488-1975. The MC3440P has three drivers with common Enable input, and one driver without Enable.



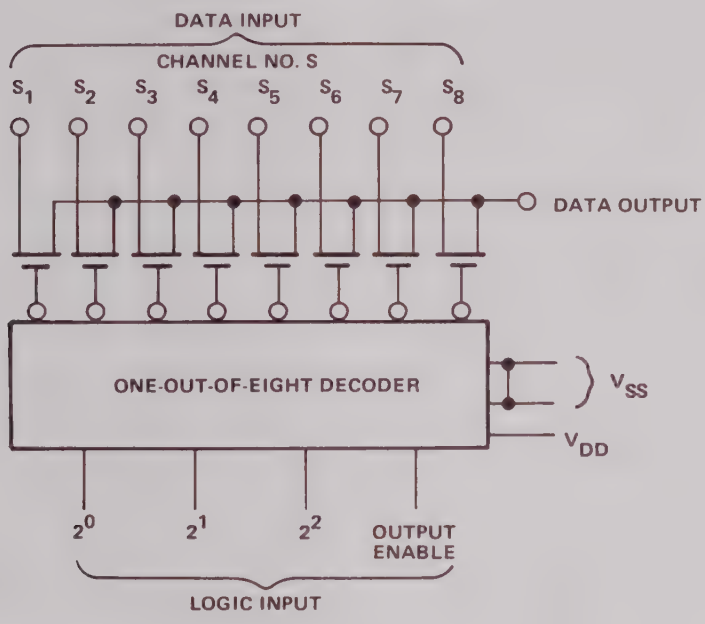


77-L-412

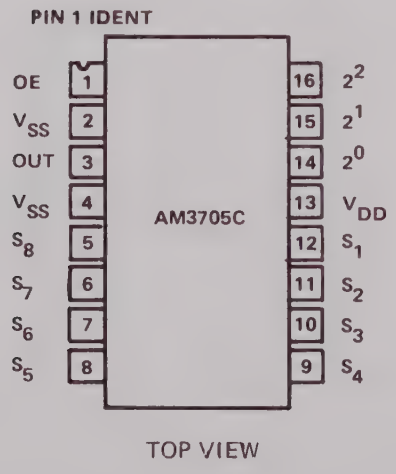
Figure 3-35. MC3440P Quad Interface Transceivers, Logic Diagram and Pin Configuration

3-70. AM3705C Analog Switch. The AM3705C (figure 3-36) is an eight-channel MOS analog multiplex switch. TTL compatible logic inputs that require no level shifting or input pull-up resistors and operation over a wide range of supply voltages is obtained by constructing the device with low threshold P-channel enhancement MOS technology. To simplify external logic requirements, a one-of-eight decoder and an output enable are included in the device.

BLOCK DIAGRAM



PIN CONFIGURATION



TOP VIEW

TRUTH TABLE

LOGIC INPUTS				CHANNELS
2^0	2^1	2^2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

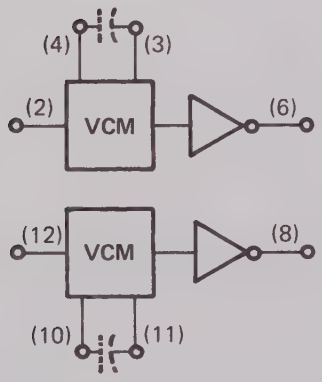
79-L-014

Figure 3-36. AM3705 Analog Switch, Block Diagram and Pin Configuration

3-71. MC4024 Voltage Controlled Multivibrator. The MC4024 (figure 3-37) is a dual voltage-controlled multivibrator that provides appropriate level shifting to produce an output compatible with TTL logic levels. Frequency control is accomplished with voltage variable current sources that control the slew rate of a single capacitor. Variation of the output frequency over a 3.5 to 1 range is possible with an input dc control voltage of +1.0 to +5 volts. The operating frequency range of this multivibrator is controlled by the value of an external capacitor. The maximum operating frequency of this device is typically 30 MHz. Three power supply and three ground connections are provided in this circuit. Each multivibrator has a separate power supply and ground connection. The output buffers have a common power supply and ground pin. This provides isolation between VCMs and minimizes the effect of output buffer transients on the multivibrators in critical applications. This separation of power supply and ground lines also provides the capability of disabling one VCM by disconnecting its Vcc to TTL logic levels.

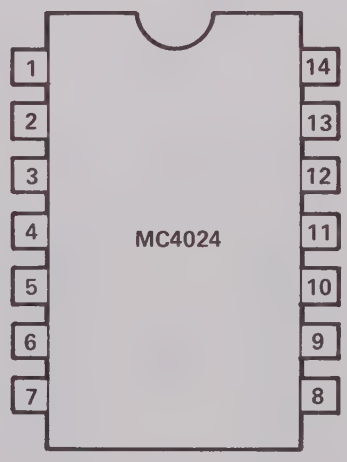
3-72. NE5534T Operational Amplifier. The NE5534T (figure 3-38) is a high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as 741 and 301A, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths. The op amp is internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc).

LOGIC DIAGRAM



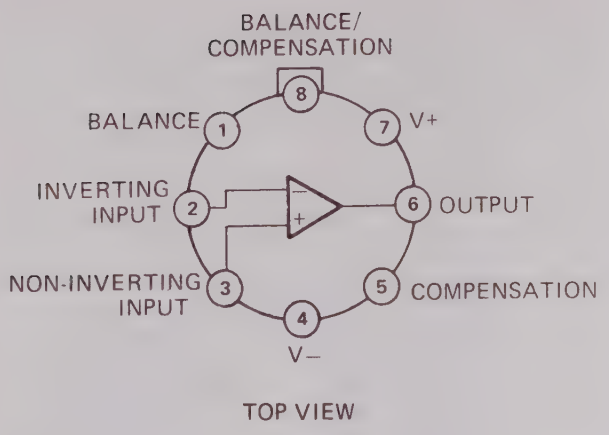
V_{CC} VCM 1,13
OUTPUT BUFFER = 14
GND VCM = 5, 9
OUTPUT BUFFER = 7
EXTERNAL CAPACITOR FOR
FREQUENCY RANGE DETERMINATION
OUTPUT LOADING FACTOR = 7
POWER DISSIPATION=150 mW typ/pkg
MAXIMUM OPERATING FREQUENCY = 30 MHz typ

PIN CONFIGURATION



77-L-414

Figure 3-37. MC4024 Voltage Controlled Multivibrator, Logic Diagram and Pin Configuration

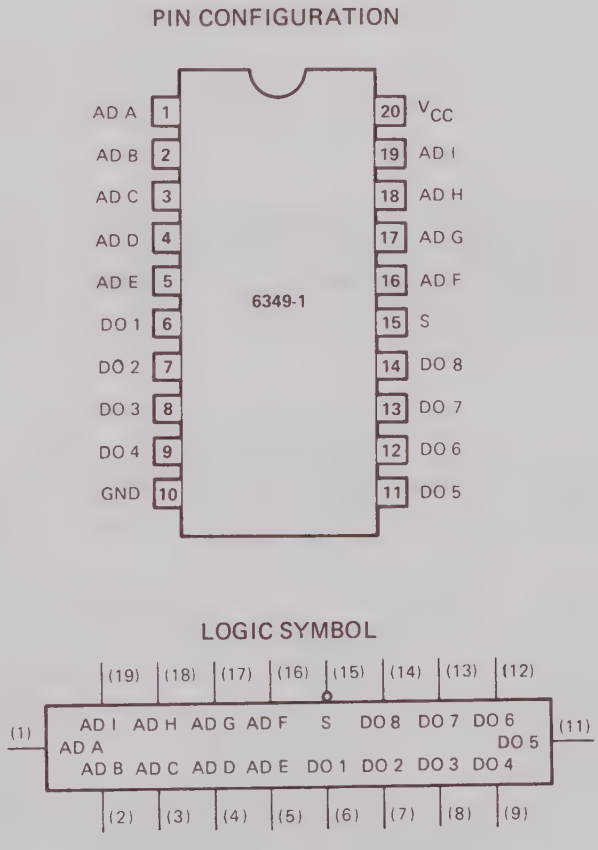


79-L-025

Figure 3-38. NE5534T Operational Amplifier, Pin Configuration

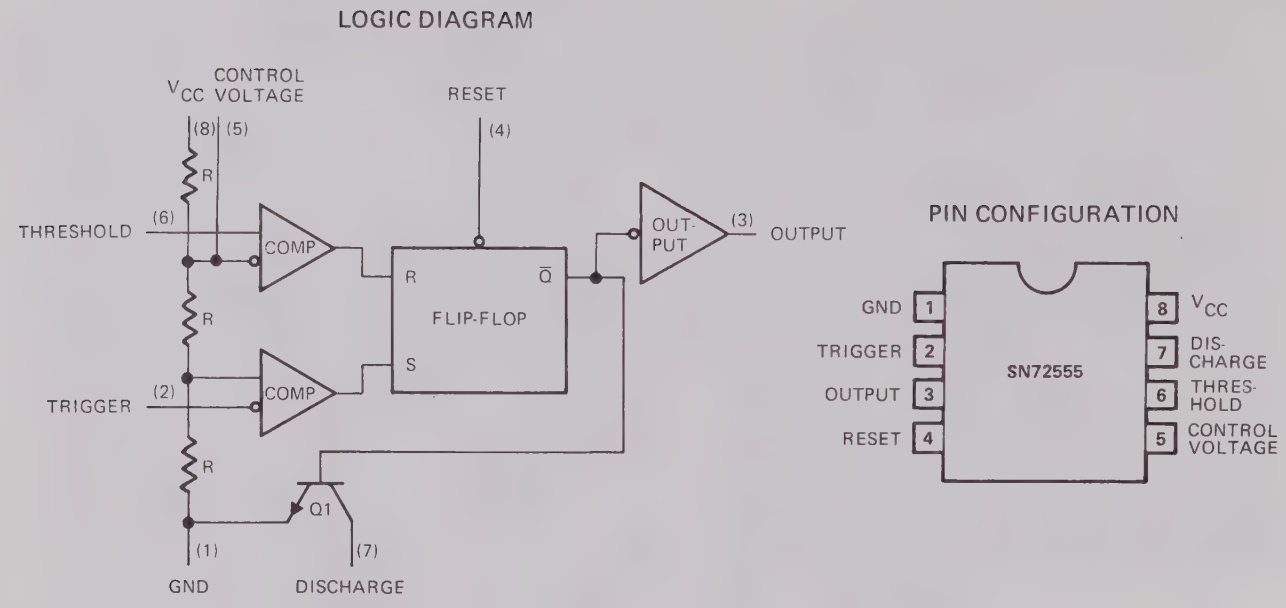
3-73. 6349-1 PROM. The 6349-1 (figure 3-39) is a three-state output programmable read only memory (PROM). This 4k, 20 pin PROM has absolute maximum ratings of -0.5 to 7.0V supply voltage; -1.5 to +5.5V input voltage; -20mA to 5mA input current; ±100mA output current, and -65 to +150 degrees Celsius storage temperature. It has an operating temperature range of 0 to +70 degrees Celsius.

3-74. SN72555N Timer. The SN72555 (figure 3-40) is a monolithic timing circuit capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor. The threshold and trigger levels are normally two-thirds and one-third, respectively, of Vcc. These levels can be altered with the control voltage terminal. When the trigger input rises above the threshold level, the flip-flop is set and the output goes high. When the input rises above the threshold level, the flip-flop is reset and the output goes low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. When the output is low, a low impedance path is provided between the discharge terminal and ground. The output circuit is capable of sinking or sourcing current up to 200 milliamperes. Operation is specified for supplies of 5 to 15 volts. With a 5 volt supply, output levels are compatible with TTL inputs.



77-L-415

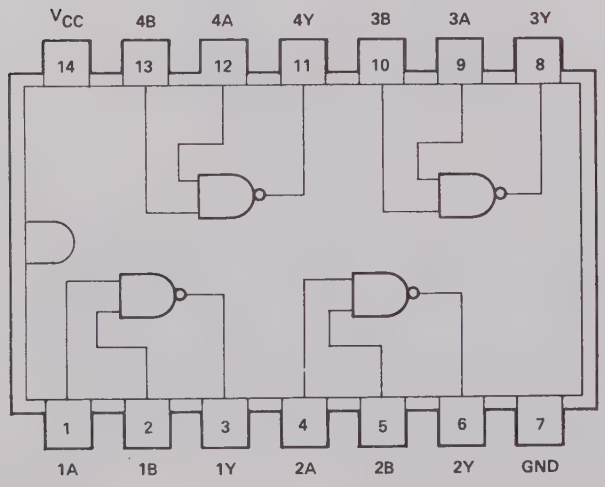
Figure 3-39. 6349-1 PROM, Pin Configuration



77-L-416

Figure 3-40. SN72555N Precision Timer, Logic Diagram and Pin Configuration

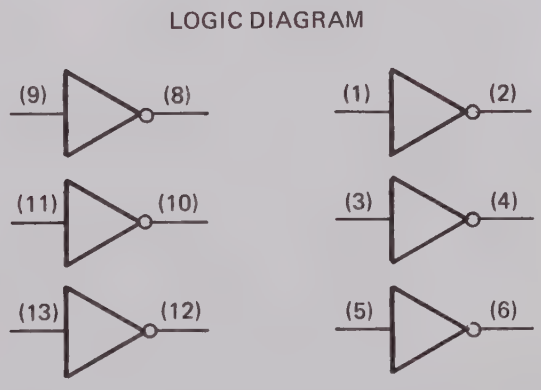
3-75. SN74LS00N Quad NAND Gates. The SN74LS00N (figure 3-41) consists of four 2-input NAND gates in a DIP package. The logic function it performs is shown in figure 3-9.



79-L-016

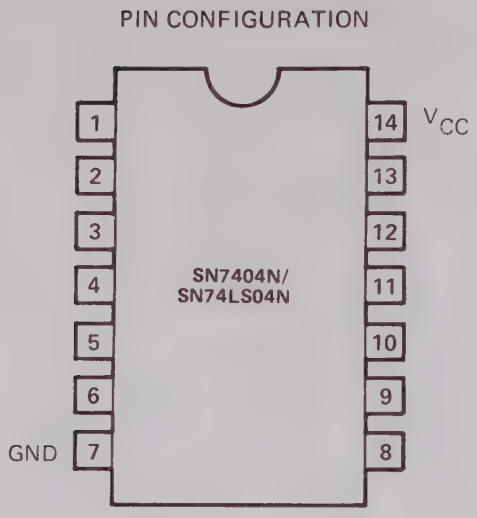
Figure 3-41. SN74LS00N Quad NAND Gates, Pin Configuration

3-76. SN7404N and SN74LS04N Hex Inverters. The SN7404N and the SN74LS04N (figure 3-42) are hex inverters that use TTL to achieve high speed at nominal power dissipation. It has input clamping diodes and a typical noise immunity of one volt, fanout of 10, and allowable power supply variation of 4.75 volts to 5.25 volts.



77-L-417/1

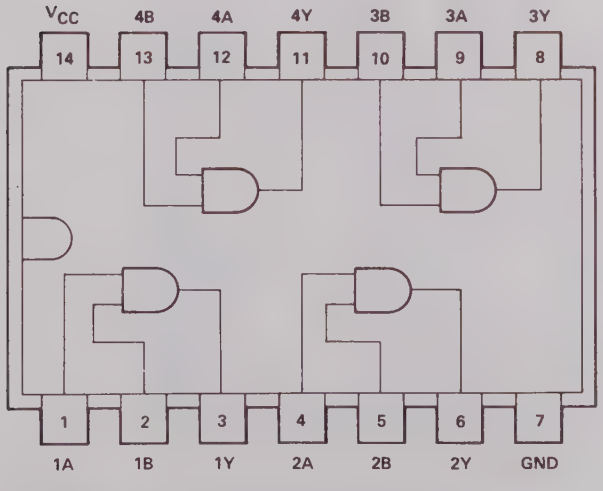
Figure 3-42. SN7404N and SN74LS04N Hex Inverters, Pin Configuration (Sheet 1 of 2)



77-L-417/2

Figure 3-42. SN7404N and SN74LS04N Hex Inverters, Pin Configuration (Sheet 2 of 2)

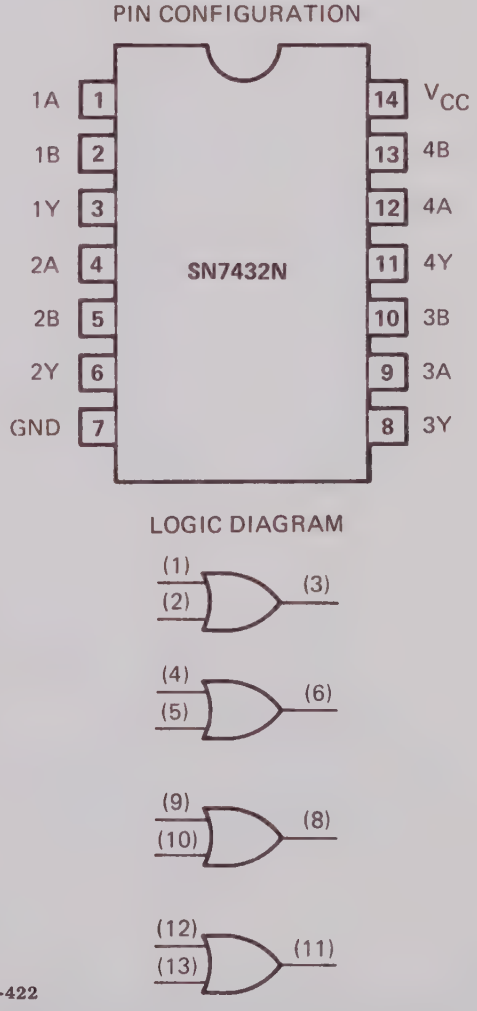
3-77. 7408 Series AND Gates. There are three types of AND gates in the WJ-1204: SN7408N, SN74LS08N, and SN74L09N (figure 3-43). They are all quad two-input AND gates in a DIP package. The logic functions they perform are shown in figure 3-9. The differences among them are in their performance specifications, not their function.



79-L-015

Figure 3-43. Quad Two-Input NAND Gates, Pin Configuration

3-78. SN7432N Quad OR Gates. The SN7432N (figure 3-44) is a quad 2-input OR gate using TTL to provide the basic functions used in the implementation of digital integrated circuit systems. Supply voltage is 7 V, input voltage is 5.5 V, and output voltage is 5.5 V, all absolute maximum ratings. The operating temperature range is -55 to +125 degrees Celsius.



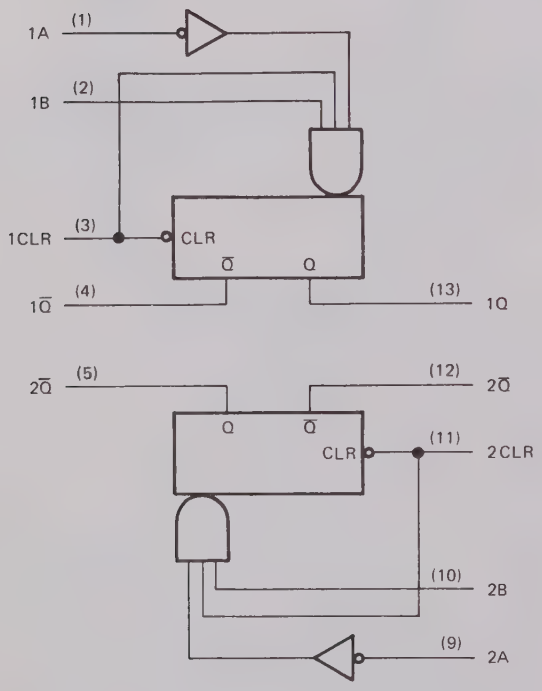
77-L-422

Figure 3-44. SN7432N Quad Two-Input OR Gates, Pin Configuration

3-79. SN74LS123N Monostable Multivibrator. The SN74LS123N (figure 3-45) is a retriggerable monostable multivibrator. The dc triggered multivibrator pulse width is controlled by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values. It has enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

3-80. SN74LS124N Dual VCO. The SN74LS124N (figure 3-46) is a dual voltage-controlled oscillator (VCO) with two independent oscillators in a single monolithic chip. The output frequency of each VCO is established by a single external component, either a capacitor or a crystal, in combination with two voltage sensitive inputs, one for frequency range and one for frequency control. The oscillator can be set to operate at any frequency between 0.12 Hz and 30 MHz and can operate from a single 5-volt supply. The enable input of this device starts or stops the output pulses when it is low or high respectively. The internal oscillator of the SN74LS124N runs continuously even while the output is disabled. The pulse synchronization-gating section ensures the first output pulse is neither clipped nor extended. Duty cycle of the squarewave

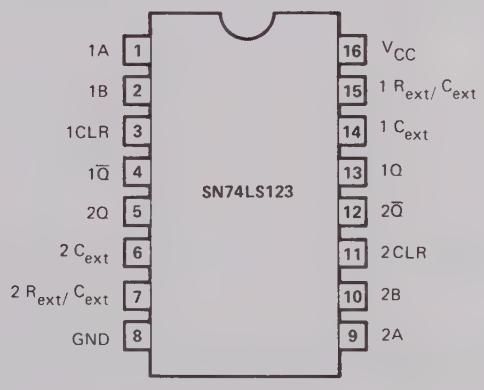
LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

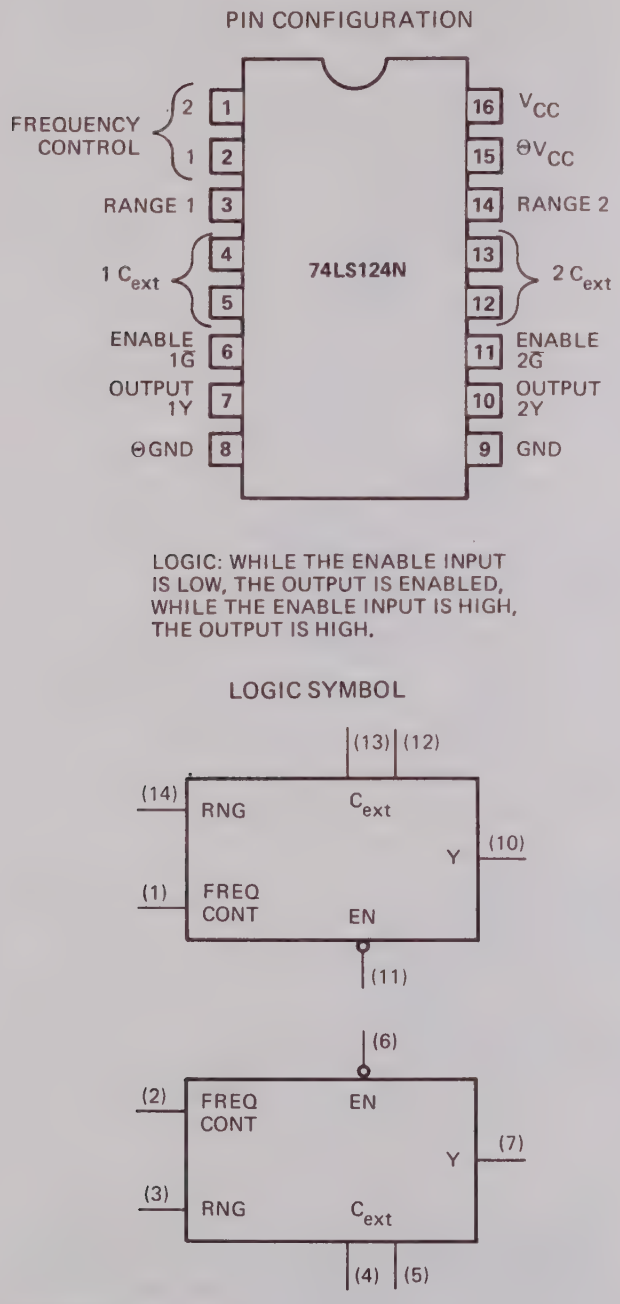
PIN CONFIGURATION



77-L-438

Figure 3-45. SN74LS123N Dual Retriggerable Monostable Multivibrator, Function Diagram

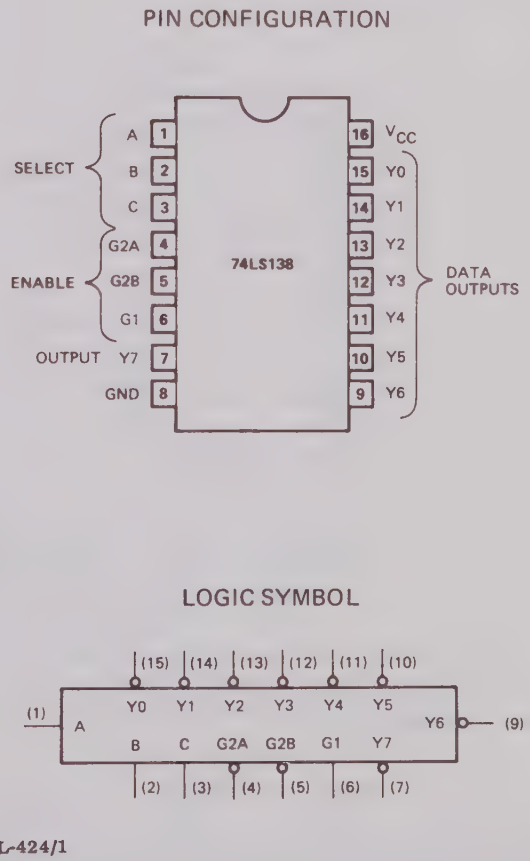
output is fixed at approximately 50 percent. Simultaneous operation of both VCOs in the same package is not recommended.



77-L-423

Figure 3-46. SN74LS124N Dual Voltage Controlled Oscillator, Pin Configuration

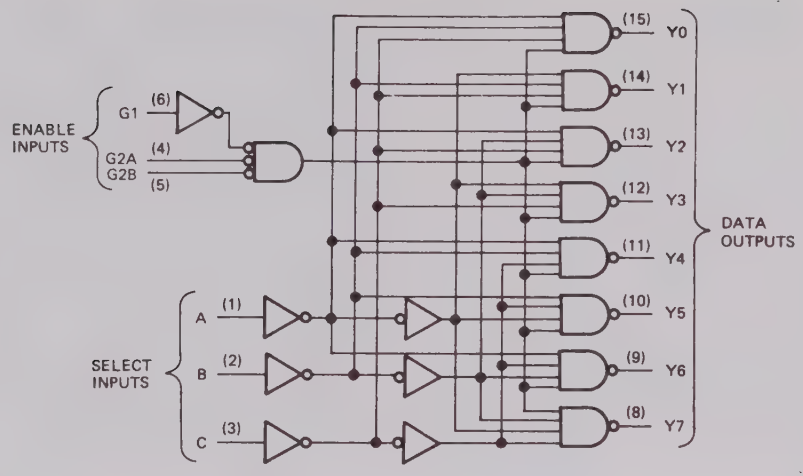
3-81. SN74LS138N Decoder/Multiplexer. The SN74LS138N (figure 3-47) is a schottky-clamped TTL MSI circuit used in memory decoding or data-routing requiring very short propagation delay times. It decodes one-of-eight lines depending on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24 line decoder can be implemented without external inverters and a 32 line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.



77-L-424/1

Figure 3-47. SN74LS138N 3-to-8 Line Decoder/Multiplexer, Function Diagram (Sheet 1 of 2)

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

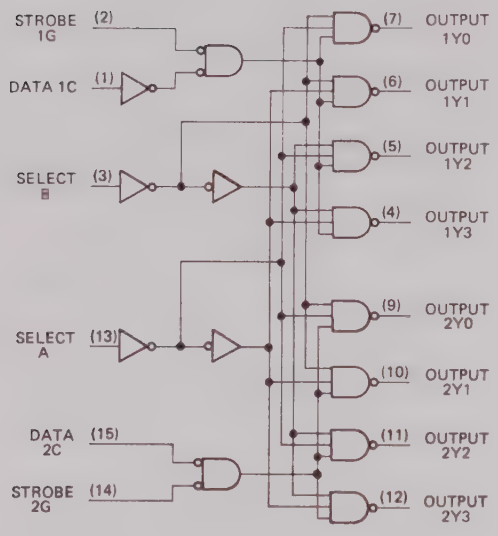
77-L-424/2

Figure 3-47. SN74LS138N 3-to-8 Line Decoder/Multiplexer, Function Diagram (Sheet 2 of 2)

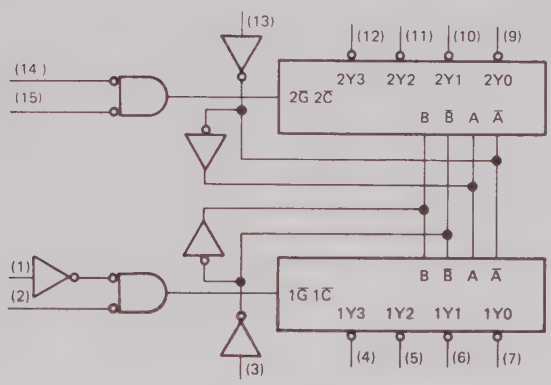
3-82. SN74LS156N Decoder/Multiplexer. The SN74LS156N (figure 3-48) is dual 2-line-to-4-line decoder/demultiplexer with individual strobes and common binary address inputs in a single 16 pin package. When both sections are enabled by the strobes, the common binary address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is

inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating.

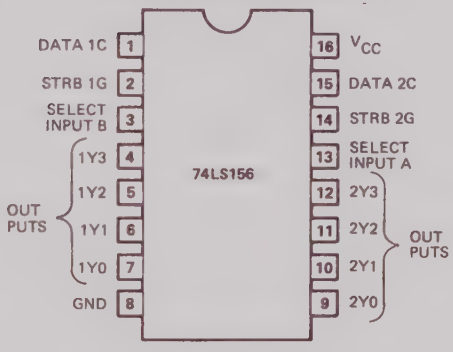
LOGIC DIAGRAM



LOGIC SYMBOL



PIN CONFIGURATION



FUNCTION TABLE
3-LINE-TO-8LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

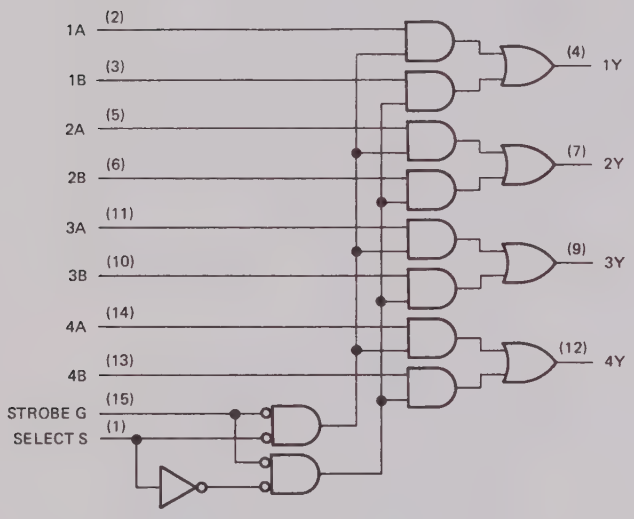
†C = Inputs 1C and 2C connected together
‡G = Inputs 1G and 2G Connected Together
H = High Level, L = Low Level, X = Irrelevant

77-L-425

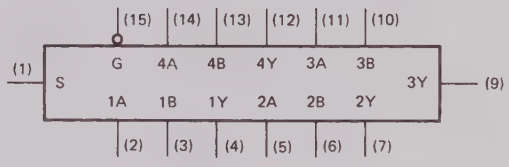
Figure 3-48. SN74LS156N Decoder/Multiplexer, Function Diagram

3-83. SN74LS157N Data Selector. The SN74LS157N (figure 3-49) is a quadruple 2-line-to-1-line data selector/multiplexer. It contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

LOGIC DIAGRAM



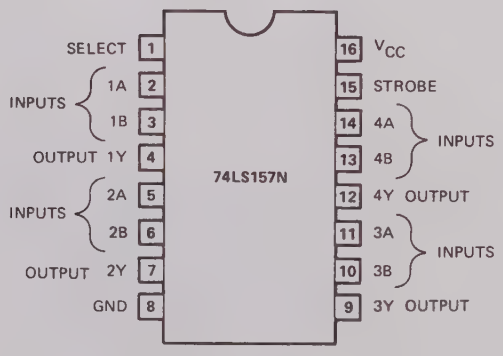
LOGIC SYMBOL



FUNCTION TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	'157,'L157 'LS157,'S157
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

PIN CONFIGURATION

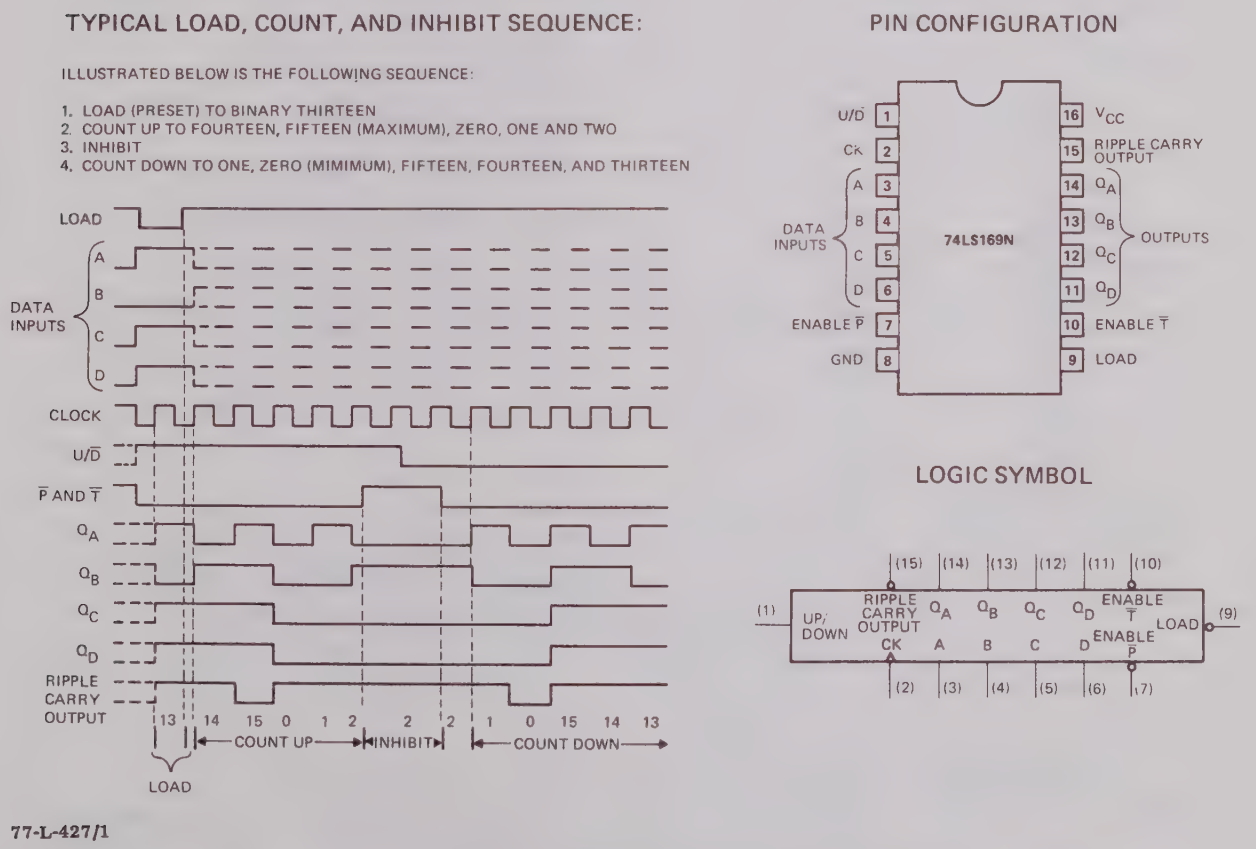


POSITIVE LOGIC:
LOW LEVEL AT S SELECTS A INPUTS
HIGH LEVEL AT S SELECTS B INPUTS

77-L-426

Figure 3-49. SN74LS157N Quad 2-to-1-Line Data Selector, Function Diagram

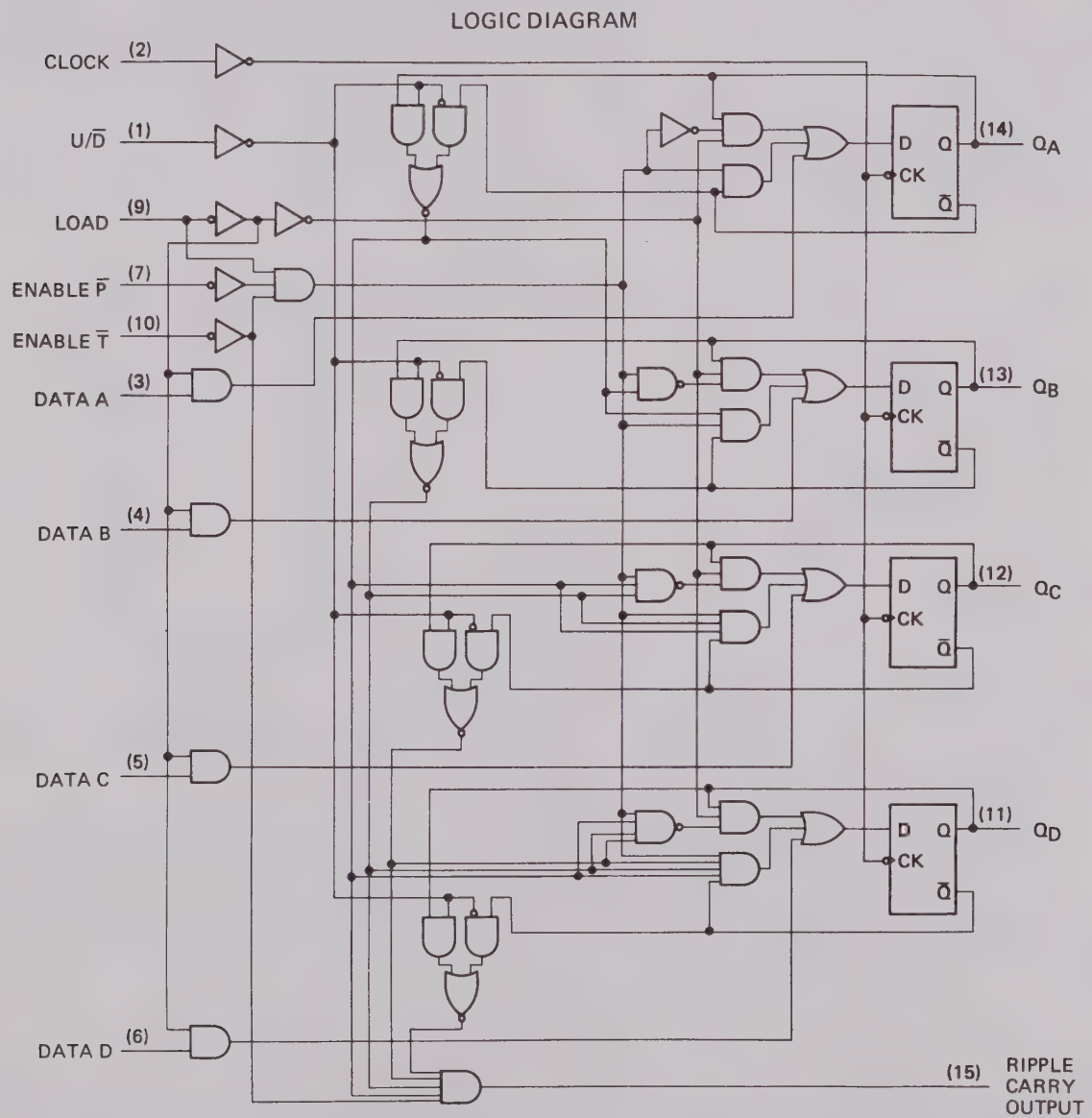
3-84. SN74LS169N Up/Down Synchronous Counter. The SN74LS169N (figure 3-50) is a synchronous presettable binary counter with an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other on instruction from the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform. These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input T is fed forward to enable the carry output. The carry output thus enabled



77-L-427/1

Figure 3-50. SN74LS169N 4-Bit Up/Down Synchronous Counter, Function Diagram (sheet 1 of 2)

will produce a low-level output pulse with a duration approximately equal to the high portion of the QA output when counting up and approximately to the low portion of the QA when counting down. This low-level overflow carry pluse can be used to enable successive cascaded stages.Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. The SN74LS169N has a fully independent clock circuit. Changes at control inputs (Enable $\overline{P}$, Enable $\overline{T}$, Load, Up/$\overline{Down}$) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

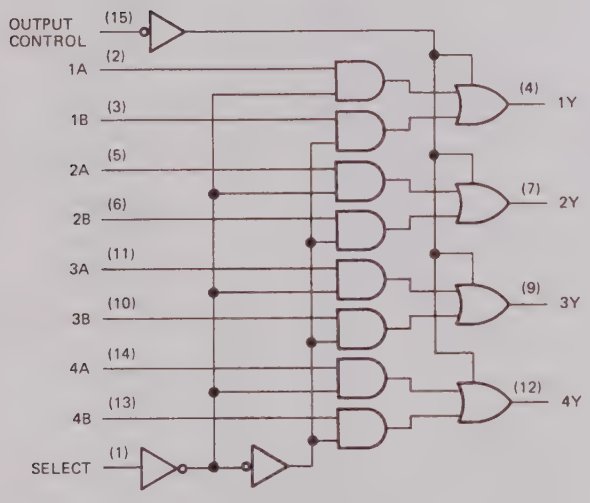


77-L-427/2

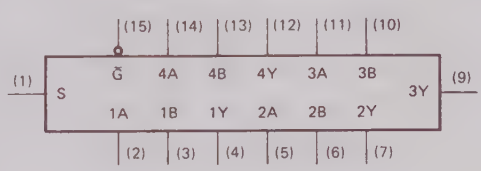
Figure 3-50. SN74LS169N 4-Bit Up/Down Synchronous Counter, Function Diagram (sheet 2 of 2)

3-85. SN74LS257N Data Selector/Multiplexer. The SN74LS257N (figure 3-51) is a quadruple 2-line-to-1-line data selector/multiplexer. It is a Schottky-clamped high performance multiplexer with three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed so that the output disable times are shorter than the output enable times. This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

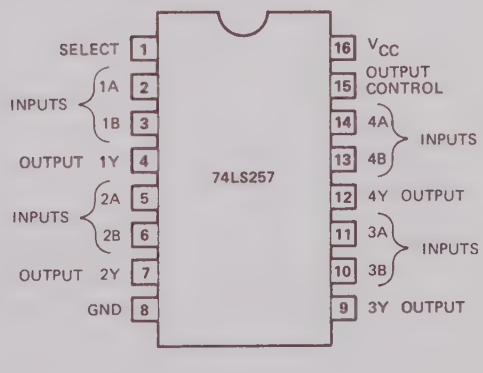
LOGIC DIAGRAM



LOGIC SYMBOL



PIN CONFIGURATION



FUNCTION TABLE

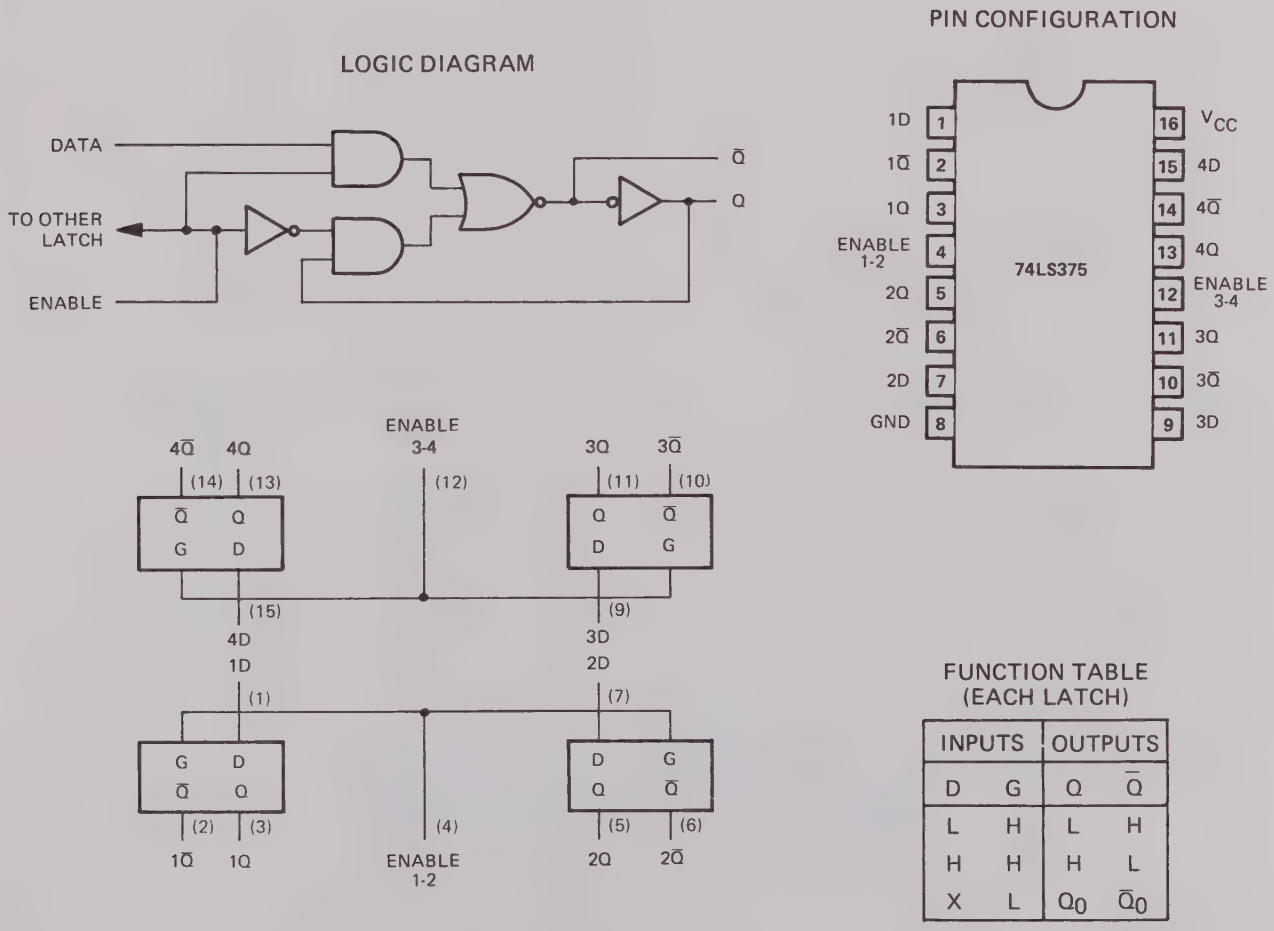
INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	'LS257A 'S257
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

77-L-428

Figure 3-51. SN74LS257N Quad Data Selector/Multiplexer Function Diagram

3-86. SN74LS375N Bistable Latches. The SN74LS375N (figure 3-52) is a 4-bit bistable latch used for temporary storage of binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

3-87. 8216 Bidirectional Bus Driver. The 8216 (figure 3-53) is a 4 bit parallel bidirectional bus driver/receiver. All inputs are low power TTL compatible. All outputs may be tri-stated.



FUNCTION TABLE (EACH LATCH)

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

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Figure 3-52. SN74LS375N 4-Bit Bistable Latches, Function Diagram

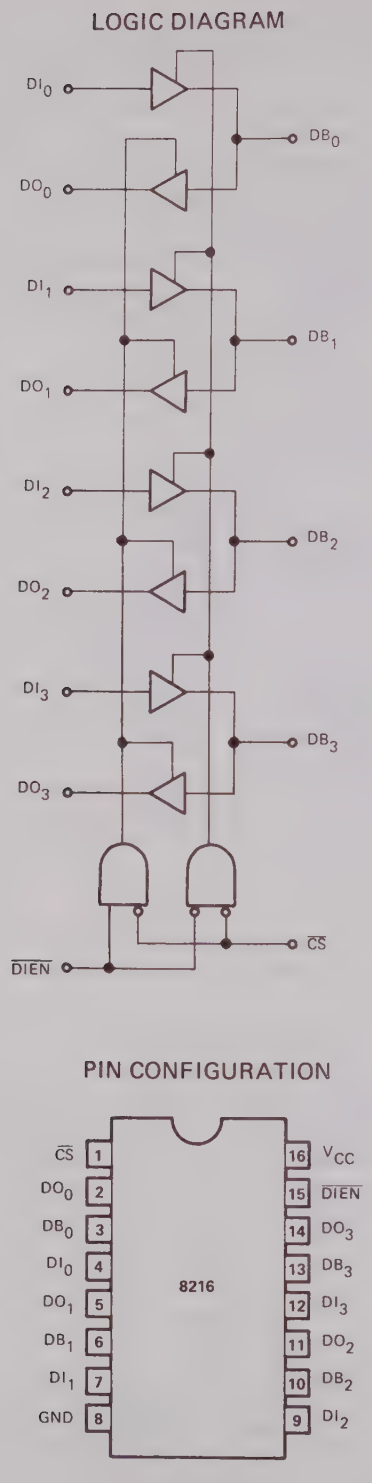

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Figure 3-53. 8216 Bidirectional Bus Driver, Logic Diagram and Pin Configuration

3-88. 8255A Programmable Peripheral Interface. The 8255A (figure 3-54) programmable peripheral interface (PPI) is a tri-state, bidirectional, eight-bit device designed for interfacing peripheral equipment to the system bus. It accepts input from the CPU Address, Data, and Control busses. A low on the chip select ($\overline{CS}$) input enables the communication between the 8255A and the CPU. A low on the read ($\overline{RD}$) input pin enables the 8255A to send the Data or Status information to the CPU. A low on the write ($\overline{WR}$) input pin enables the CPU to write Data or Control words into the 8255A. Address lines A_0 and A_1, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports of the Control Word Register. A high on the reset (RESET) input clears all internal registers including the Control Resiser and all ports (A,B,C) are set to the input mode. The functional configuration of each port of the 8255A is programmed by the system software. In essence the CPU outputs a control word during the power-up cycle that contains information such as mode, bit set, bit reset, etc., that initializes the functional configuration of the 8255A. Each of the Control blocks (Group A and Group B) accepts commands from the Read/Write Control logic, receives control words from the internal data bus and issues the proper commands to its associated ports. The Control Word Register can only be written into. No read operation of the Control Word Register is allowed. All three ports (A,B, and C) can all be configured in a wide variety of functional characteristics by system software, but each has its own special features.

3-89. SP8602A and SP8604B Counters. The SP8602A and SP8604B (figure 3-55) are fixed-ratio ECL divide-by-two counters with maximum specified input (I/P) frequencies of 500 MHz (for SP8602A) and 300 MHz (for SP8604B). The counter can be operated with single input drive or with double, complementary, input drive. The input is normally capacitively coupled to the signal source. Two complementary emitter follower outputs are provided. The signal

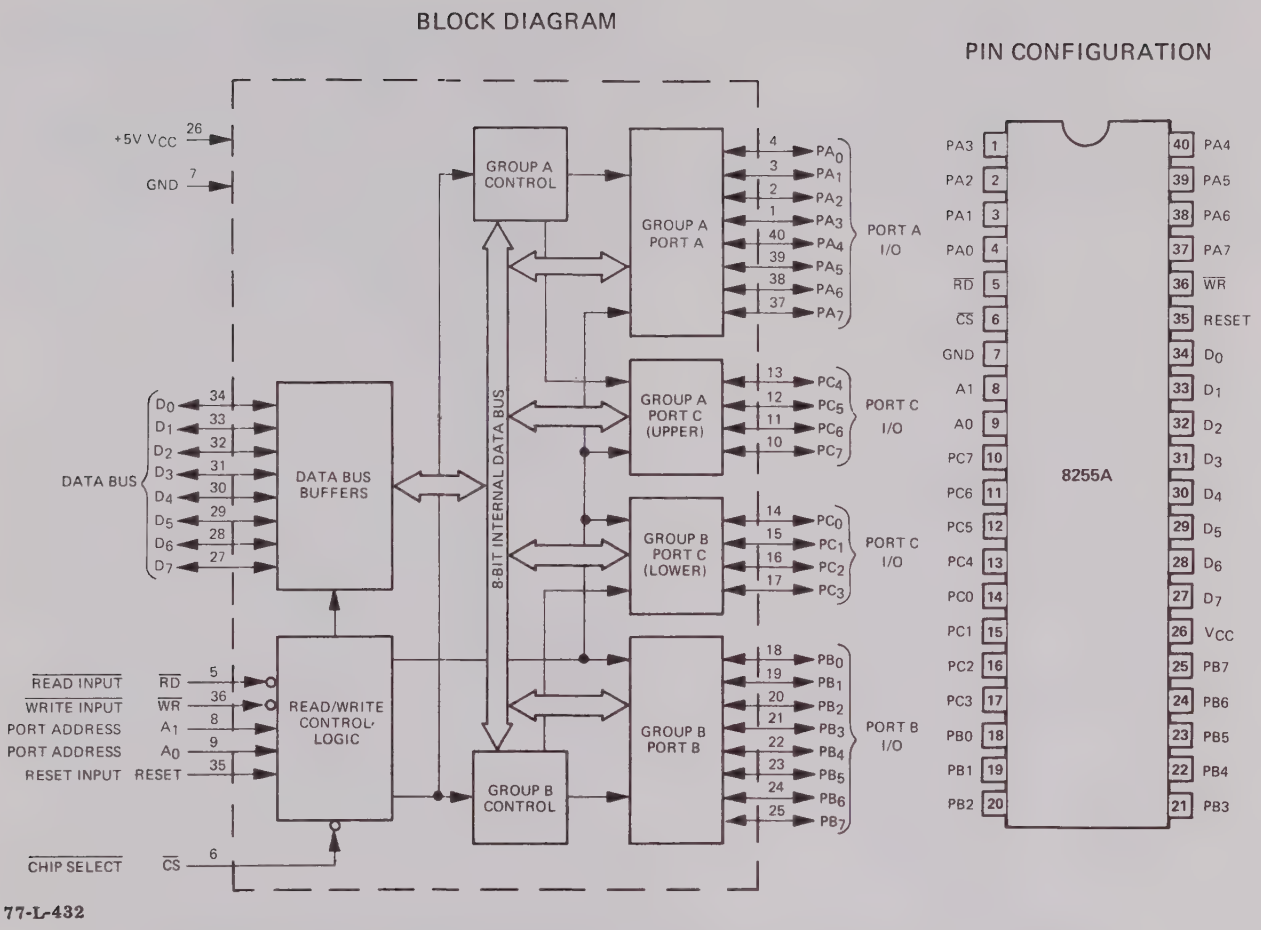

Figure 3-54. 8255A Programmable Peripheral Interface, Block Diagram and Pin Configuration

source is normally capacitively coupled to the input. The input waveform may be sinusoidal, but below about 40 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than the amplitude. A square wave input with a slew rate of more than 100 V per microsecond will permit correct operation down to dc.

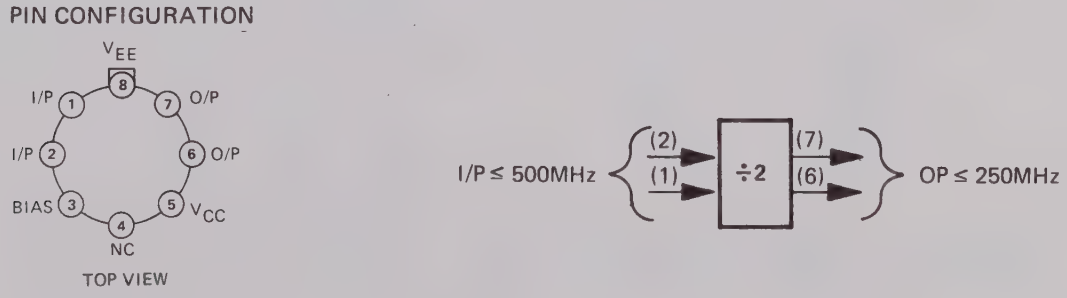

Figure 3-55. SP8602A and SP8604B ECL Counters, Pin Configuration

3-90. SP8609B Counter. The SP8609B (figure 3-56) is a fixed-ratio divide-by-two asynchronous ECL counter with a maximum operating frequency in excess of 1 GHz over a temperature range of 0 to +70 degrees Celsius. The input can be capacitively coupled to the signal source or dc coupled if required. The two complementary emitter follower outputs are capable of driving 100 ohm lines and interfacing to ECL with the same positive supply. The 8609B requires supplies of 0 V and -7.4 V (± 0.4 V). In the absence of an input signal both the dc coupled and the capacitively coupled circuits will self oscillate with an output frequency of approximately 200 MHz. This can be prevented by connecting a 10 kilohm resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100 millivolts. The SP8609B will miscount with low frequency sinewave inputs or slow ramps. A slew rate of 200V per microsecond or greater is necessary for safe operation at low frequencies.

3-91. F95010 Decade Counter. The F95010 (figure 3-57) is a high speed, synchronous, presettable, and cascadable BCD decade counter. Typical count frequency is 200 MHz. It is capable of assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count (TC) is generated internally in a manner that allows synchronous reading at nearly the speed of the basic counter. The device is specified for operation over the temperature range of zero to +75 degrees Celsius.

3-92. F95105DC and F95109DC OR/NOR Gate. The F95105DC and the F95109DC (figure 3-58) are ECL OR/NOR gates with an operating temperature of 0 to 75 degrees Celsius. Propagation Delay (Low to High and High and Low) and Output Transistion Time (Low to High and High to Low) are typically 2.0 nanoseconds.

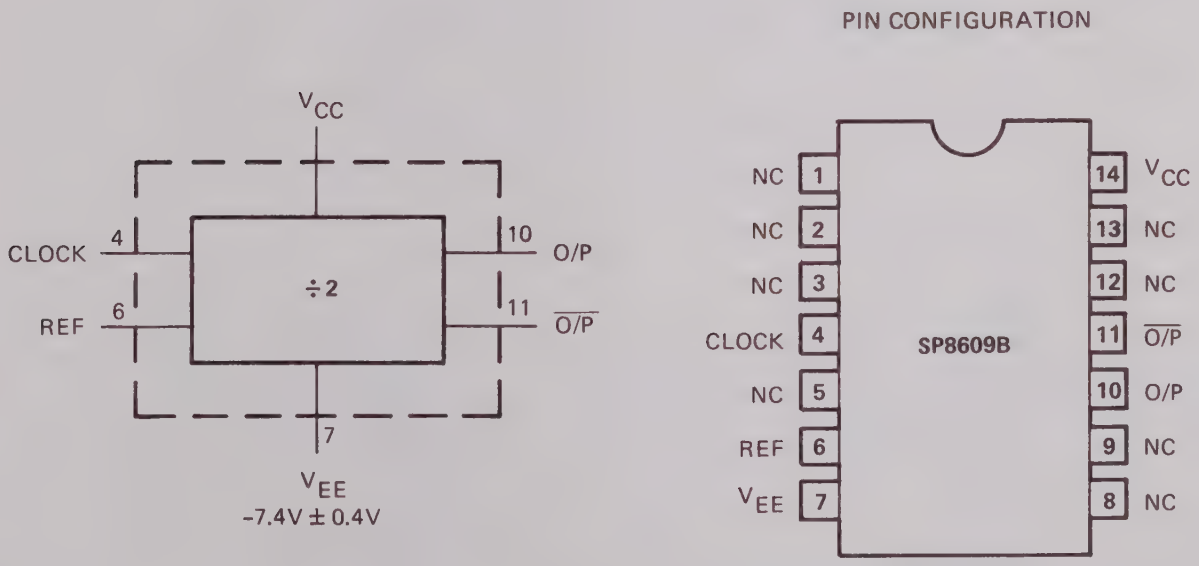

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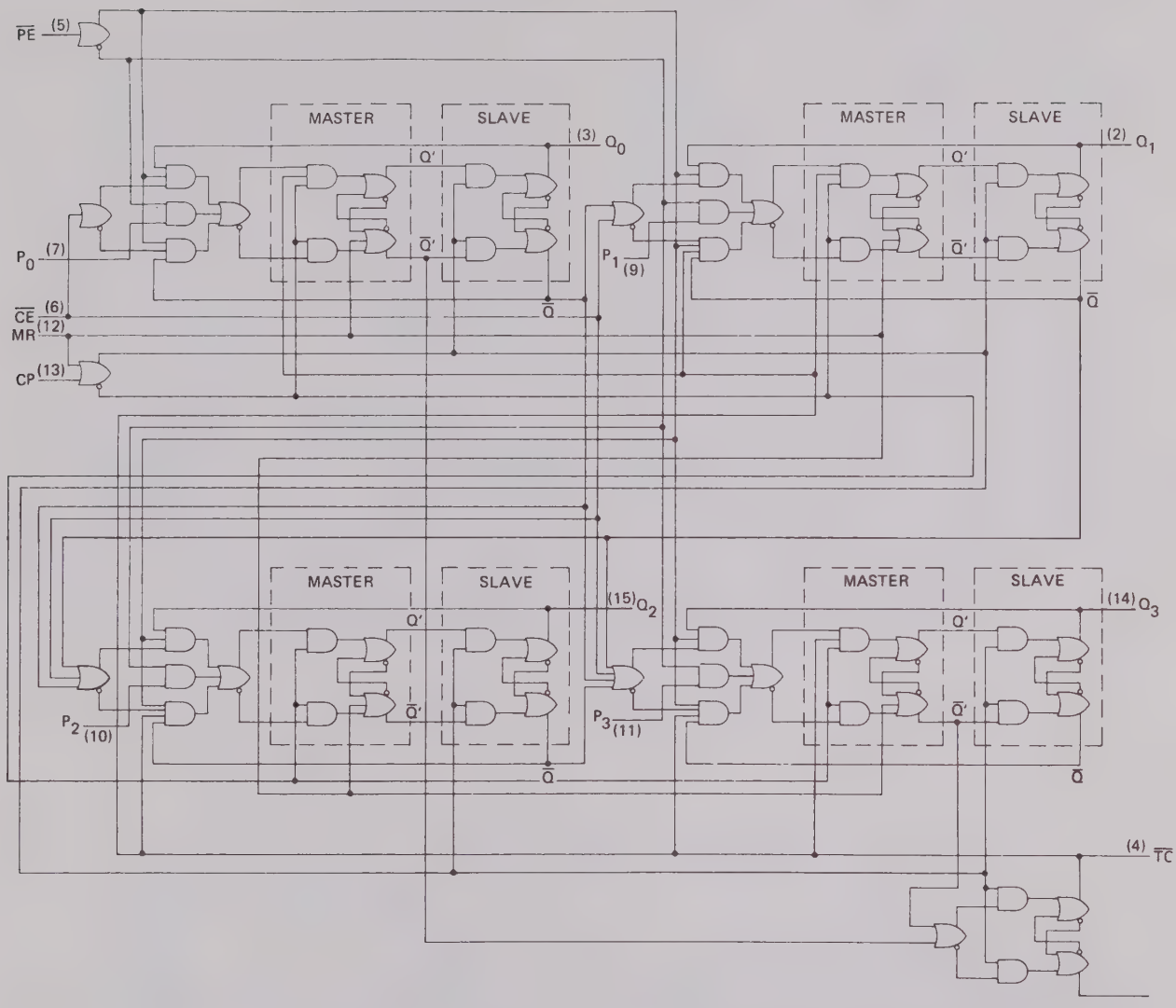
Figure 3-56. SP8609B ECL Counter, Pin Configuration

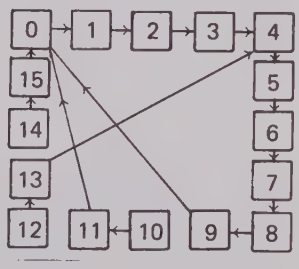
LOGIC DIAGRAM



FUNCTION TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	↑	Load Parallel (P_n to Q_n)
H	L	L	↑	Load Parallel (P_n to Q_n)
L	H	L	↑	Count
H	H	L	↑	Hold
X	X	L	↓	Masters Respond, Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{TC}$ = HIGH)

STATE DIAGRAMS



NOTE: The 95010 can be preset to any state, but will not count beyond 9 (HLLH). If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

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Figure 3-57. F95010 BCD Decade Counter, Function Diagram

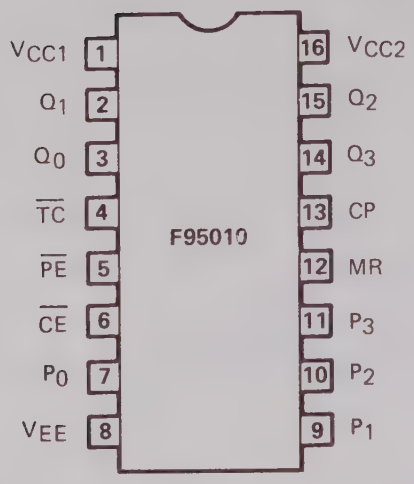
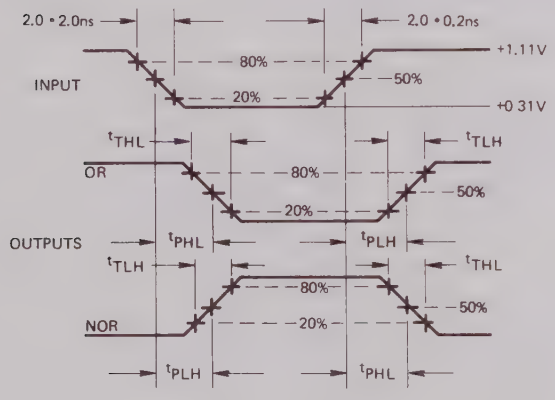


Figure 3-57. F95010 BCD Decade Counter, Function Diagram (sheet 2 of 2)

3-93. 96L02 Multivibrator. The 96L02 (figure 3-59) is a TTL, monostable, low power, dual retriggerable, resettable, monostable multivibrator that provides an output pulse with duration and accuracy that is a function of external timing components. The 96L02 has excellent immunity to noise on the Vcc and ground lines. The 96L02 uses TTL inputs and outputs for high speed and has high fan-out capability.

3-94. MC12040L Phase-Frequency Detector. The MC12040L (figure 3-60) is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. It determines the "lead" or "lag" phase relationships and the time difference between two waveforms. The phase error information is contained in the output duty cycle. Phase detector gain is approximately 0.16 volts/radian.



FUNCTION TABLE

A	B	OUTPUT	$\overline{\text{OUTPUT}}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

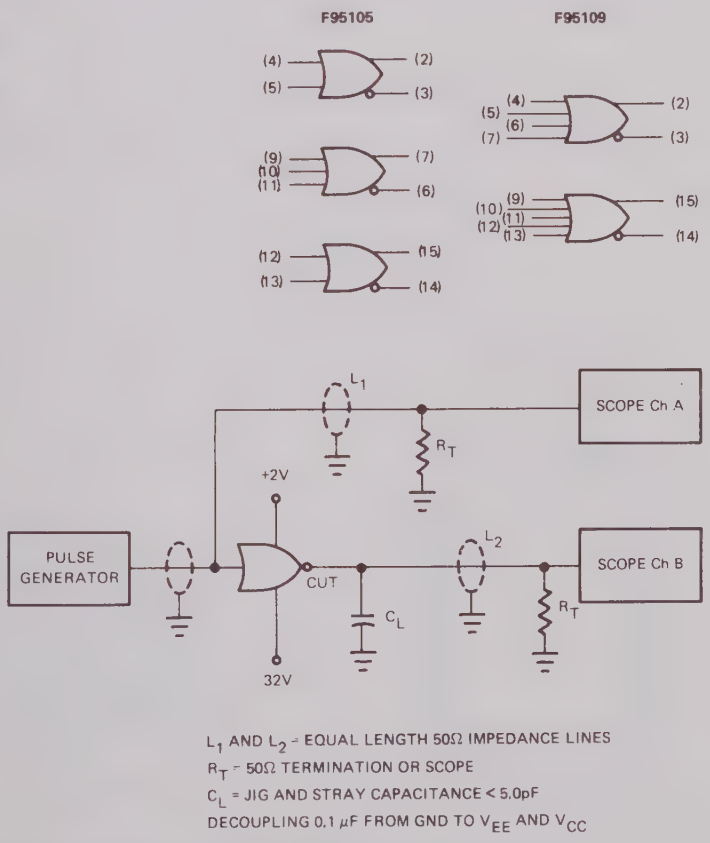


Figure 3-58. F95105DC and F95109DC OR/NOR Gates, Function Diagram

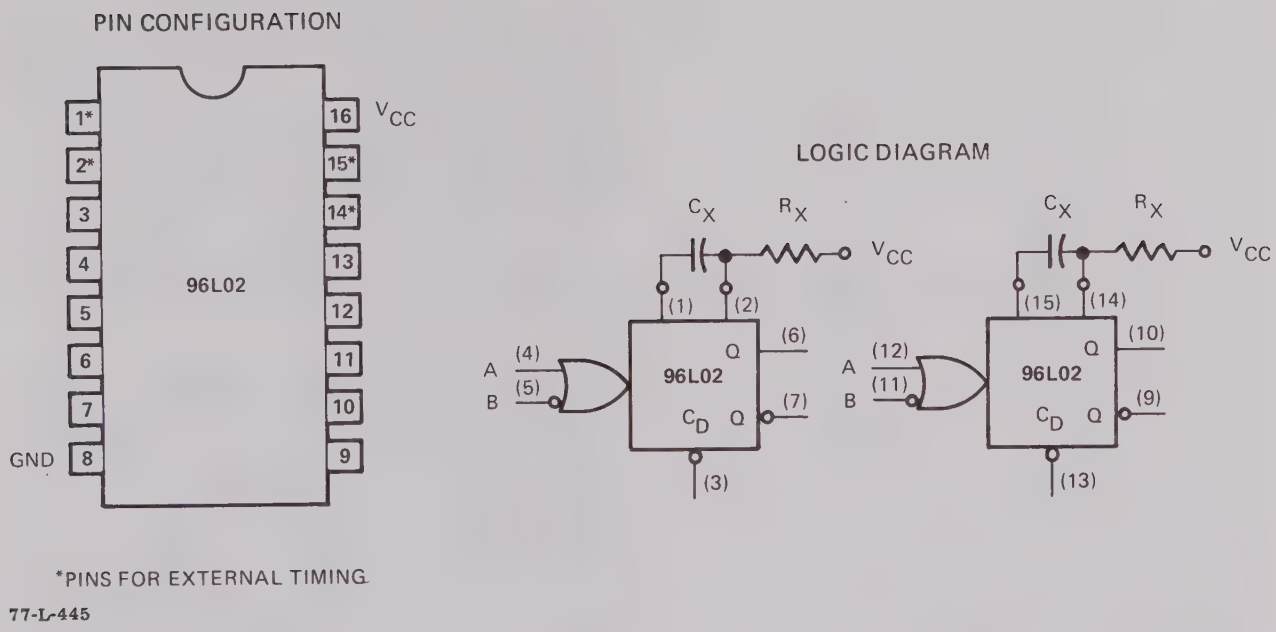


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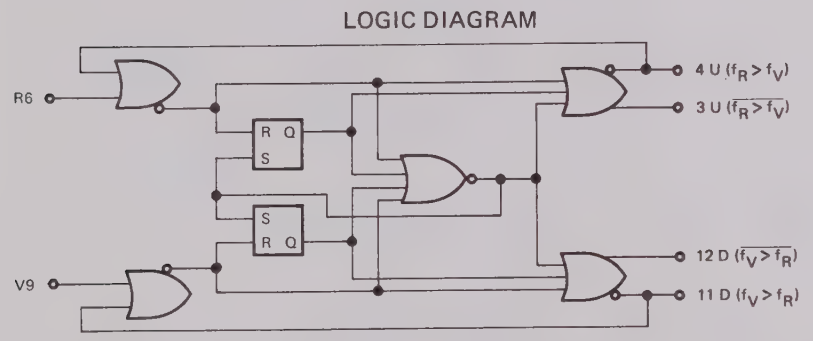
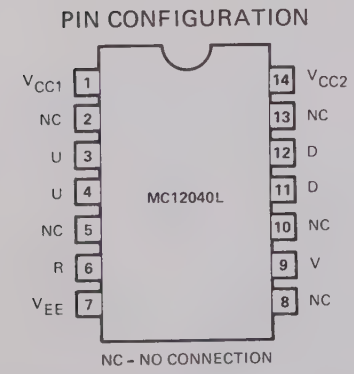
Figure 3-59. 96L02 Dual Retriggerable Multivibrator, Logic Diagram and Pin Configuration





77-L-408

TRUTH TABLE

This is not strictly a functional truth table, i.e., it does not cover all possibile modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

FUNCTION TABLE

INPUT		OUTPUT			
R	V	U	D	$\overline{U}$	$\overline{D}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	0

Figure 3-60. MC12040L Phase-Frequency Detector, Function Diagram

3-95. 784-1-R3.3K Resistor Network. The 784-1-R3.3K (figure 3-61) is a Single-In-Line package containing seven 3.3 kilohm resistors. Resistance tolerance is ± 2% (± 2 ohms) and package power rating at +25°C is 2.1 watts. Its operating temperature range is -65°C to +125°C.

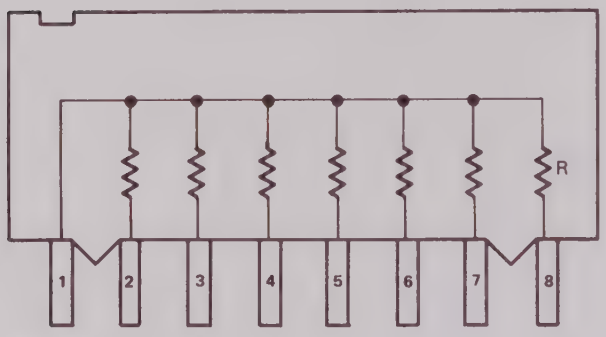


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Figure 3-61. 784-1-R3.3K Resistor Network, Pin Configuration

3-96. 898-3-R220 Resistor Network. The 898-3-R220 (figure 3-62) is a resistor network consisting of eight 200 ohm resistors in a DIP package. Resistance tolerance is ±2% (±2 ohms), and package power rating at +25°C is 1.5 watts maximum.

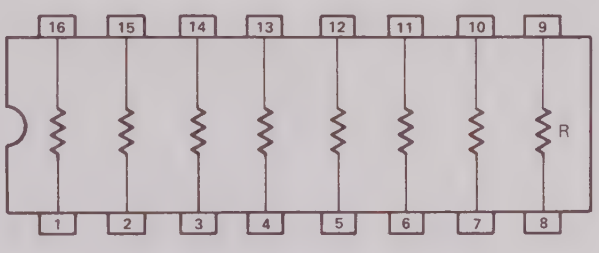

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Figure 3-62. 898-3-R220 Resistor Network, Pin Configuration

MAINTENANCE

CHAPTER 4

SCHEDULED MAINTENANCE

4-1. INTRODUCTION. This chapter contains scheduled maintenance procedures for the WJ-1204-1 Synthesized Signal Generator. Included is a scheduled maintenance action index; preventive maintenance procedures including cleaning, servicing, preservation, and lubrication instructions; and scheduled performance test instructions.

4-2. SCHEDULED MAINTENANCE ACTION INDEX. The scheduled maintenance action index is provided in table 4-1. This table lists all maintenance actions described in this chapter in alphanumeric order. In column one (Periodicity), the following symbols are used:

Symbol	Interval
D	Daily
W	Weekly
M	Monthly
Q	Quarterly
S	Semiannually
A	Annually
R	Recommended (as specified)

4-3. The Maintenance Action column lists the maintenance action which corresponds to the periodicity number in column 1. The Reference column states the paragaph number that contains the procedure listed in column 2.

4-4. EQUIPMENT REQUIRED. Table 4-2 is a list of equipment required for performing preventive maintenance and performance test procedures. The first column gives the nomenclature of the equipment. (Refer to table 1-3 for applicable equipment parameters.)

4-5. PREVENTIVE MAINTENANCE PROCEDURES. The following preventive maintenance procedures provide cleaning, inspection, preservation, and lubrication instructions for the WJ-1204-1.

Table 4-1. Scheduled Maintenance Action Index

Periodicity							Maintenance action	Reference
D	W	M	Q	S	A	R		
		X					Cleaning	Paragraph 4-6
			X				Inspection	Paragraph 4-7
					X	X	Performance Test	Paragraph 4-8

WARNING

Do not clean or inspect the interior of the equipment with the power cord plugged in. Under certain conditions, dangerous voltage potentials may exist when the power control is in the OFF position, due to charges retained by capacitors. Always remove power and discharge or ground a circuit before touching it.

4-6. Cleaning. All parts and connectors should be free of dirt, dust, corrosion, or other foreign matter. Remove dust from surfaces by directing a stream of dry, fil tered, compressed air at an angle of 45 degrees to the surface being cleaned. Use a soft brush to remove particles not removed by compressed air. Clean assemblies as follows:

CAUTION

Do not use water, solvent, or gasoline to clean circuit cards, terminals, or switches.

a. Ensure that all chassis power has been removed.

b. Remove top cover of chassis to provide access to internal components.

c. Remove dust and dirt with a vacuum cleaner. Use a dry 1/2 - inch wide paint brush to remove dust from corners.

d. Wipe all exposed surfaces with a cloth moistened in isopropyl alcohol. Other cleaning materials, approved for military use, may be used without harming parts or finish if used in accordance with label instructions. Circuit cards may be cleaned with trichloroethane (table 4-3).

Table 4-2. Tools and Test Equipment Required

Nomenclature	Qty	Intended use
Spectrum analyzer	1	Performance test
Power meter	1	Performance test
Frequency counter	1	Performance test
Power head	1	Performance test
Detector	1	Performance test
Function generator	1	Performance test
Oscilloscope	1	Performance test
Vacuum cleaner	1	Cleaning interior of unit
Brush, 1/2 inch wide	1	Cleaning interior of unit

WARNING

Observe the following precautions when using isopropyl alcohol or trichloroethane: Use with adequate ventilation. Avoid prolonged or repeated contact with skin. Avoid prolonged breathing of vapors. Do not take internally. Keep container closed. Keep away from heat and open flames.

e. Reinstall covers removed in step b.

4-7. Inspection. Check connectors and mountings for tightness. Check cables for fraying or other damage. Check all terminals for tightness and see that corrosion has not formed under hardware. Perform the following service:

a. Examine handles for sturdy mounting.

b. Examine chassis for loose, cracked, or broken parts.

c. Examine resistors for bulging, discoloration, and broken or corroded solder connections.

d. Examine semiconductors and integrated circuits for cracks and for corroded, loose, or broken pins and connectors.

e. Examine wiring for discolored, cracked, or frayed insulation and loose or broken connections.

f. Examine cabling for frayed, loose, or broken lacing.

CAUTION

Indiscriminate inspection of connectors can be detrimental. A representative, random selection, based upon equipment environment and maintenance history should suffice. If corrosion is detected, all associated connectors must be examined.

g. Examine jacks, plugs, and terminals for corrosion and broken connections.

h. Examine circuit card receptacles for cracks and corrosions.

i. Examine all connections to microwave devices for loose, broken, or corroded connections.

Table 4-3. Recommended Cleaning Solutions

Nomenclature	Federal stock number (FSN)	Applicable specifications	Intended use
1,1,1-trichloroethane, inhibited, vapor degreasing	6810-00-551-1487	O-T-620C, MIL-T-81533A	Clean circuit boards, chassis
Isopropyl alcohol	6505-00-205-6513	TT-I-735a	Clean circuit boards, chassis

4-8. SCHEDULED PERFORMANCE TEST. The performance test consists essentially of the maintenance turn-on procedure described in paragraph 5-15. The maintenance turn-on procedure, and thus the performance test, ensures that the equipment is operating within intended performance standards and that corrective action isolates trouble to a particular assembly. Failure to obtain the required performance standard is usually due to a specific circuit malfunction. When all performance standards are obtained, the unit is functioning correctly and may be returned to service.

CHAPTER 5

TROUBLESHOOTING

5-1. INTRODUCTION. This chapter provides detailed information on troubleshooting the WJ-1204-1 Synthesized Signal Generator. Included is a troubleshooting index, a protective device index, maintenance turn-on procedures, troubleshooting procedures, schematic and logic diagrams, and power distribution diagrams.

5-2. Proper maintenance of the Synthesized Signal Generator requires a familiarity with both normal and abnormal indications based upon a complete knowledge and understanding of equipment operational characteristics (chapter 1) and functional theory (chapter 3). Full use of available diagrams of the WJ-1204 can be a useful tool in locating potential sources of an equipment malfunction. A logical procedure should be followed in troubleshooting when abnormal indications are noted during equipment operation. Troubleshooting procedures should be based on the eight logical steps described in the following paragraphs.

5-3. Determining The Problem. The first step in troubleshooting any electronic equipment is to determine what the problem is. Generally the problem is evident but be certain you understand it clearly. By performing the maintenance turn-on procedure, you can usually determine which section of the instrument is malfunctioning.

5-4. Listing Probable Faulty Functions. After determining and confirming the problem, think about it, using logical reasoning. The maintenance technician should be thoroughly familiar with chapters 2 and 3 in order to analyze the symptoms observed during the maintenance turn-on procedure. Formulate a number of "logical choices" as to the cause and likely location of the trouble. These choices are mental decisions which are based on knowledge of the equipment operation, a full identification of the trouble symptom, and information contained in this manual. It may be useful to refer to the Troubleshooting Index table or the Troubleshooting Procedure table when selecting possible faulty sections.

5-5. Physical Inspection. Before servicing the equipment, go over the equipment using your physical senses to detect faulty conditions. Visual inspection of such items as loose or damaged cabling, connectors, or circuit cards should be made. Listen for any strange sounds; smell for unusual odors; feeling for overheated parts should only be done by experienced, competent, and knowledgable technicians, if at all.

5-6. Isolating The Faulty Section. This step involves the use of test equipment. For the greatest efficiency in localizing trouble, the functional sections which have been selected by the "logical choice" method should be tested in an order that requires the least amount of time. This requires a mental selection to determine which section to test first. The selection should be based on the validity of the "logical choice" and the difficulties in making the necessary tests. If the tests do not prove that functional section to be at fault, the next selection should be tested, and so on, until the faulty functional section is located.

5-7. Localizing The Defective Stage. After the faulty functional section has been isolated, it is often necessary to make additional "logical choices" as to which circuit or group of circuits (within the functional

section) is at fault. Look at the input and output waveforms of each stage. When you find missing or erroneous waveforms, the defective stage has been located. Once the defective stage has been pinpointed, further tests are necessary to determine the defective circuit and part or parts. Servicing block diagrams, schematic diagrams, and interconnection diagrams provide the signal flow and test locating information needed to locate the faulty circuit.

5-8. Failure Analysis. After the trouble (faulty component, stage, etc.) has been located (but prior to taking corrective action), the procedures followed up to this point should be reviewed to determine why the fault affected the equipment in the manner that it did. This review is usually necessary to make certain that the fault discovered is actually the cause of the malfunction, and not merely the result of the malfunction.

5-9. Replace Faulty Part. Once the faulty part has been located, it is then necessary to replace the defective component or correct the abnormal condition. Because most parts in the WJ-1204-1 are not repairable they must be replaced with the exact replacement part. Chapter 6 gives procedures for removing and reinstalling major components in the WJ-1204-1.

5-10. Test Operation. Always test for proper operation once the fault has been corrected. "Cook" the equipment for as long as necessary until absolutely sure that the defect has been repaired. Many electronic troubles have a way of fixing themselves temporarily, giving the troubleshooter a false sense of accomplishment. Be especially wary when you are not sure what you did to make the equipment return to normal operation.

5-11. TROUBLESHOOTING INDEX. Table 5-1 is a troubleshooting index that references essential information for all functional areas of the WJ-1204-1 which may require servicing.

5-12. INDICATOR LAMP INDEX. Table 5-2 provides pertinent information for all indicators on the WJ-1204-1.

Table 5-1. Troubleshooting Index

Functional area	Troubleshooting reference	Troubleshooting diagram (Fig. No.)	Functional description paragraph	Alignment/ adjust paragraph
Frequency selection	Table 5-5, Step 4, 5, 6	5-5, 5-7	3-8	6-3,6-4, 6-12
Leveling	Table 5-5, Steps 23, 24, 25	5-4	3-7	6-9
Modulation	Table 5-5, Steps 34, 35	5-4	3-7	6-6
Power measurement	Table 5-5, Steps 22, 30, 31	5-1, 5-4 5-6	3-7	6-5

Table 5-2. Indicator Lamp Index

Reference designation	Functional name	Energizing voltage	Troubleshooting diagram (Fig. No.)
DS1	UNLEVELED indicator	+5 Vdc	5-2

5-13. PROTECTIVE DEVICE INDEX. Table 5-3 provides essential information for all protective devices in the WJ-1204-1.

5-14. TYPE SMA CONNECTOR NOTES. When connecting type SMA fittings together, careful insertion of the center pin should first be made. The connector coupling nut should then be hand-tightened to be just snug. Finally, tightening torque should be applied in the range of 10 $\pm$2 inch-pounds.

5-15. MAINTENANCE TURN-ON PROCEDURES. Table 5-4 lists the procedures to energize the WJ-1204-1 from a fully de-energized condition to full operation. This procedure will enable the technician to determine which major function or supporting function is malfunctioning. Each step of the procedure includes the action to be taken, observation to be made, and a reference to the procedure in table 5-5 (troubleshooting) if the observation is out of tolerance. Each step of the procedure assumes that normal conditions have been observed in the previous steps.

5-16. TROUBLESHOOTING PROCEDURES. Table 5-5 lists most symptoms which may be encountered during an equipment malfunction. Further information includes the probable cause of the malfunction and the recommended corrective action to be taken. Reference should be made to the schematic diagrams while troubleshooting or performing any test on the equipment.

5-17. DIAGRAMS. Figures 5-1 through 5-9 provide schematic diagrams for the WJ-1204-1 as listed in table 5-6. (Circuit card assemblies are non-repairable and their schematics are provided FOR REFERENCE ONLY.)

Table 5-3. Protective Device Index

Reference designation	Panel marking	Rating		Circuit protected	Troubleshooting diagram (Fig. No.)
		Volts	Amps		
F1	FUSE	125	3	Power supply and TWTA	5-1

Table 5-4. Maintenance Turn-On Procedure

Step	Observe	Table 5-5 reference
1. Equipment required: 1 Spectrum analyzer 1 Power meter 1 Frequency counter 1 Power head 1 Detector 1 Function generator 1 Oscilloscope		
2. Preliminary procedure		
a. Position the following controls on the front and rear panels as follows: CONTROL — SETTING 5 MHz reference select — INT OUT POWER — OFF Modulation select — OFF MODE — F PROGRAM/DISPLAY — F INCREMENT — 10 MHz ATTENUATION — 0 LEVEL — Midrange		
b. Check to ensure that instrument is properly installed as described in chapter 8.		
c. Connect the frequency counter to the RF OUT port.		

Table 5-4. Maintenance Turn-On Procedure-Continued

Step	Observe	Table 5-5 reference
3. Set POWER switch to ON position.	a. Numeric LED displays are on.	a. Step 1.
	b. Frequency display shows 1.0000 GHz.	b. Step 2.
4. Allow a 10-15 minute warm-up period.		
5. Momentarily press the CAL switch, then release it.	a. RF power displayed is 00.0 ±0.1 dBm while CAL switch is pressed.	a. Step 3.
6. Using keyboard, program and enter the following frequencies:	a. Frequency displayed agrees with programmed frequency.	a. Steps 4 through 12 as applicable.
	b. Frequency displayed by counter is within 0.00035% of programmed frequency as follows:	

Programmed frequency (GHz)	Upper limit	Lower limit
0.1001	0.10010035	0.100099649
0.12499	0.124990437	0.124989562
0.12501	0.125010437	0.125009562
0.24999	0.249990875	0.249989125
0.25010	0.250100875	0.250099124
0.49990	0.499901749	0.499898250
0.50010	0.500101750	0.500098250
0.99990	0.999903500	0.999896500
1.0001	1.000103500	1.000096500
1.9999	1.999907000	1.999893000
2.0010	2.001007004	2.000992997
3.9990	3.999013997	3.998986004
4.0010	4.001014004	4.000985997
7.9990	7.999027997	7.998972004
8.0010	8.001028004	8.000971997
12.999	12.9990455	12.9989545
13.001	13.0010455	13.0009545
17.999	17.999063	17.998937
18.001	18.001063	18.000937
25.999	25.999091	25.998909

Table 5-4. Maintenance Turn-On Procedures-Continued

Step	Observe	Table 5-5 reference
7. Press RST on keyboard.	a. Frequency displayed is 1.0000 GHz.	a. Step 13.
	b. Frequency counter displays 1.0000 GHz ± 0.05 MHz.	
8. Program and enter 10.000 GHz.		
9. On keyboard press UP key and release quickly.	a. Frequency displayed on front panel and frequency counter is 10.010 GHz ± 0.5 MHz.	a. Step 14.
10. Press UP key again, but hold key in.	a. Frequency increases at 10 MHz increments.	a. Step 14.
11. Press DWN key until 8.000 GHz is reached.	a. Frequency decrements in 10 MHz steps.	a. Step 15.
12. Program 28 GHz and enter.	a. Frequency displayed on unit is 28.000 GHz and flashes off and on.	a. Step 16.
	b. Frequency counter displays 8.0000 GHz ± 0.5 MHz.	b. Step 16.
13. Press CLR key.	a. Frequency displayed is 8.000 GHz.	a. Step 17.
14. Set PROGRAM/DISPLAY switch to START.	a. Unit displays 1.0000 GHz. (The display flashes when the start frequency is higher than the stop frequency.)	a. Step 18.
15. Program 13.000 GHz and enter.		
16. Set PROGRAM/DISPLAY switch to STOP.	a. Unit displays 2.0000 GHz.	a. Step 19.
17. Program 18.000 GHz and enter.		
18. Set PROGRAM/DISPLAY switch to F.		

Table 5-4. Maintenance Turn-On Procedures-Continued

Step	Observe	Table 5-5 reference
19. Set MODE switch to SWEEP.	a. The frequency is sweeping from 13.000 GHz to 18.000 GHz in 10 MHz increments.	a. Step 20, 21.
20. Set INCREMENT switch to 100 MHz position.	a. The frequency increments in 100 MHz steps. (This may be difficult to observe since the total sweep will take 2 seconds.)	a. Step 21.
21. Set INCREMENT switch to 1 MHz position.	a. The frequency increments in 1 MHz steps.	a. Step 21.
22. Repeat steps 13 through 18 using the start and stop frequencies shown below.	a. The displayed and measured frequency sweeps the programmed limits at 1 MHz increments.	a. Step 20.
23. Set MODE switch to F.		
24. Press RST key.	a. Frequency displayed is 18.000 GHz ± 0.05 MHz.	a. Step 13.
25. Remove frequency counter, and connect power meter to RF OUT port.		

Start (GHz)	Stop (GHz)
0.10000	0.12500
0.12500	0.25000
0.25000	0.50000
0.50000	1.0000
1.0000	2.0000
2.0000	4.0000
4.0000	8.0000
8.0000	13.000
18.000	26.000

Table 5-4. Maintenance Turn-On Procedure-Continued

Step	Observe	Table 5-5 reference
26. Program the following frequencies, and adjust LEVEL potentiometer for 0 dBm output as displayed on external power meter. (For frequencies above 18 GHz, connect the power head directly to the RF OUT port.) Frequency (GHz) 0.11250 0.18750 0.37500 0.75000 1.5000 3.0000 6.0000 10.500 15.500 22.000	a. RF power displayed by WJ-1204 is within ± 1 dBm of externally measured power.	a. Steps 22 through 26 as applicable. Steps 27 through 29 as applicable.
27. Remove power meter and connect spectrum analyzer to RF OUT port.		
28. Program and enter 13 GHz.		
29. Adjust LEVEL potentiometer so that 0 dBm is displayed on spectrum analyzer.		
30. Adjust ATTENUATOR through its range.	a. Signal is attenuated approximately 10 dB for every step selected by ATTENUATOR.	a. Step 30.
31. Adjust LEVEL potentiometer from MIN to MAX positions.	a. RF power varies linearly over a 20 dB range (approximately).	a. Step 31.
32. Set MODE switch to F ± ΔF position.		

Table 5-4. Maintenance Turn-On Procedures-Continued

Step	Observe	Table 5-5 reference
33. Adjust ΔF potentiometer from MIN to MAX positions.	a. Frequency deviates about the center frequency a variable number of hertz as displayed on spectrum analyzer.	a. Steps 32, 33.
34. Remove spectrum analyzer and connect detector and oscilloscope to RF OUT port. Use SYNC OUT for oscilloscope trigger input.		
35. Set Modulation Select switch to SQUARE WAVE position.	a. The oscilloscope display is a 1 kHz square wave with a 50% duty cycle.	a. Step 34.
36. Set thumbwheel switches to 10.0 microseconds.		
37. Set Modulation Select switch to PULSE position.	a. The oscilloscope display is a 10-microsecond pulse at 1 kHz repetition rate.	a. Steps 34, 35.
38. Set thumbwheel switches to the following settings: Selected pulse width (μs) 00.1 00.5 01.0 05.0 10.0	a. The measured pulse width on the oscilloscope is within 10% of selected value.	a. Step 35.
39. Set Modulation Select switch to EXT position.		
40. Connect the function generator to the MOD IN port.		

Table 5-4. Maintenance Turn-On Procedures-Continued

Step	Observe	Table 5-5 reference
41. Set function generator to output a TTL level, 10 kHz, 50% duty cycle square wave.	a. Oscilloscope displays a 10 kHz square wave with a 50% duty cycle.	a. Step 34.

Table 5-5. Troubleshooting Procedures

Symptom	Probable cause	Corrective action
1. Unit will not turn on.	a. Open fuse F1.	a. Replace F1.
	b. Faulty power supply PS1.	b. Replace PS1.
	c. Defective input line filter A18.	c. Check circuit card in A18; replace if necessary.
	d. Defective POWER switch S1.	d. Replace S1.
	e. Disconnected, broken or loose wire from power supply.	e. Replace PS1.
2. Power-up frequency displayed is not 1.0000 GHz.	a. Faulty power supply PS1.	a. Replace PS1.
	b. Faulty ac power input.	b. Turn the unit off, then back on.
	c. Defective connection between front panel assembly and Motherboard A2.	c. Check connections for cleanliness and and for good contact.
	d. Defective Keyboard and Display Assembly A1.	d. Replace A1.
	e. Defective connection of circuit cards to Motherboard A2.	e. Check connections for cleanliness and for good contact.
	f. Defective Digital Control Assembly A5.	f. Replace A5.
	g. Defective I/O Extender A6.	g. Replace A6.
	h. Defective Motherboard A2.	h. Replace A2.

Table 5-5. Troubleshooting Procedures-Continued

Symptom	Probable cause	Corrective action
3. RF POWER will not display 00.0 ± 0.1 dBm during calibration mode.	a. Faulty connection between front panel assembly and Motherboard A2.	a. Check connections for cleanliness and for good contact.
	b. Defective CAL switch.	b. Replace switch.
	c. Defective connection between circuit cards and Motherboard A2.	c. Check connections for cleanliness and for good contact.
	d. Defective RF Control Assembly A4.	d. Replace A4.
	e. Defective Digital Control Assembly A5.	e. Replace A5.
	f. Defective I/O Extender Assembly A6.	f. Replace A6.
	g. Defective Motherboard A2.	g. Replace A2.
4. Unit will not phase-lock at any frequency.	a. Defective VCO Y1.	a. Replace Y1.
	b. Defective reference oscillator A7U20.	b. Replace A7.
	c. Defective Synthesizer Assembly A7.	c. Replace A7.
	d. Defective VCO driver circuit A2U1.	d. Replace Motherboard A2.
	e. Broken wire or defective cable.	e. Locate and repair defective part.
	f. Missing supply voltage.	f. Replace power supply.
	g. 5 MHz Reference Select switch (rear panel) is in EXT position.	g. Set switch to INT select.

Table 5-5. Troubleshooting Procedures-Continued

Symptom	Probable cause	Corrective action
	h. Defective Digital Control Assembly A5.	h. Replace A5.
	i. Defective I/O Extender Assembly A6.	i. Replace A6.
	j. Defective Motherboard A2.	j. Replace A2.
5. Unit will not phase-lock at some frequencies.	a. Defective VCO Y1.	a. Replace Y1.
	b. Defective Synthesizer Assembly A7.	b. Replace A7.
	c. Defective VCO driver circuit A2U1.	c. Replace Motherboard A2.
	d. Faulty VCO coarse tuning.	d. Perform VCO coarse tune adjustment.
	e. Missing supply voltage.	e. Replace power supply.
	f. Defective Digital Control Assembly A5.	f. Replace A5.
	g. Defective I/O Extender Assembly A6.	g. Replace A6.
6. No RF output at any frequency.	a. Faulty power supply PS1.	a. Replace PS1.
	b. Defective coaxial RF switch S11.	b. Return to depot maintenance.
	c. Defective step attenuator AT1.	c. Replace front panel assembly.
	d. Faulty Digital Control Assembly A5.	d. Replace A5.

Table 5-5. Troubleshooting Procedures-Continued

Symptom	Probable cause	Corrective action
	e. Faulty I/O Extender Assembly A6.	e. Replace A6.
	f. Faulty Synthesizer Assembly A7.	f. Replace A7.
7. No RF output below 1 GHz.	a. Defective switch/pin diode leveler S7.	a. Replace S7.
	b. Defective amplifier AR1.	b. Replace AR1.
	c. Defective switch/filter assembly A10.	c. Replace A10.
	d. Defective coaxial RF switch S11.	d. Return to depot maintenance.
	e. Defective pulse driver/modulator A9.	e. Replace A9.
	f. Faulty Digital Control Assembly A5.	f. Replace A5.
	g. Faulty I/O Extender Assembly A6.	g. Replace A6.
	h. Faulty RF Control Assembly A4.	h. Replace A4.
	i. Faulty Power Meter Assembly A3.	i. Return to depot maintenance.
8. No RF output above 1 GHz.	a. Defective switch/filter assembly A10.	a. Replace A10.
	b. Defective switch/filter assembly A12.	b. Replace A12.
	c. Defective Γ oubler A11.	c. Replace A11.
	d. Defective amplifier AR2.	d. Replace AR2.
	e. Defective coaxial RF switch S11.	e. Return to depot maintenance.

Table 5-5. Troubleshooting Procedures-Continued

Symptom	Probable cause	Corrective action
	f. Defective coaxial RF switch S10.	f. Replace S10.
	g. Faulty Digital Control Assembly A5.	g. Replace A5.
	h. Faulty I/O Extender Assembly A6.	h. Replace A6.
9. No RF output above 2 GHz.	a. Defective Switch/Filter Assembly A12.	a. Replace A12.
	b. Defective multiplier A13.	b. Replace A13.
	c. Multiplier A13 out of alignment.	c. Align A13
	d. Missing +20 Vdc from power supply PS1.	d. Replace PS1.
	e. Defective Coaxial RF switch S8.	e. Replace S8.
	f. Defective Pin Leveler A14.	f. Replace A14.
	g. Faulty Digital Control Assembly A5.	g. Replace A5.
	h. Faulty I/O Extender Assembly A6.	h. Replace A6.
	i. Defective RF Control Assembly A4.	i. Replace A4.
	j. Defective Power Meter Assembly A3.	j. Replace A3.
10. No RF output above 8 GHz.	a. Defective coaxial RF switch S8.	a. Replace S8.
	b. Defective TWTA AR3.	b. Replace AR3.
	c. Defective coaxial RF switch S9.	c. Replace S9.

Table 5-5. Troubleshooting Procedures-Continued

Symptom	Probable cause	Corrective action
	d. Faulty Digital Control Assembly A5.	d. Replace A5.
	e. Faulty I/O Extender Assembly A6.	e. Replace A6.
11. No RF output in 13 - 18 GHz range.	a. Defective Doubler/Filter Assembly A17.	a. Replace A17.
	b. Defective coaxial RF switch S9.	b. Replace S9.
	c. Defective coaxial RF switch S10.	c. Replace S10.
	d. Faulty Digital Control Assembly A5.	d. Replace A5.
	e. Faulty I/O Extender Assembly A6.	e. Replace A6.
12. No RF output above 18 GHz.	a. Defective Doubler/Filter Assembly A16.	a. Replace A16.
	b. Defective coaxial RF switch S9.	b. Replace S9.
	c. Defective coaxial RF switch S11.	c. Return to depot maintenance.
	d. Faulty Digital Control Assembly A5.	d. Replace A5.
	e. Faulty I/O Extender Assembly A6.	e. Replace A6.
13. Unit will not return to start frequency when RST key is pressed.	a. Defective RST key.	a. Replace A1.
14. Unit will not increment when UP key is pressed.	a. Defective UP key.	a. Replace A1.
	b. Faulty Keyboard and Display Assembly A1.	b. Replace A1.

Table 5-5. Troubleshooting Procedures-Continued

Symptom	Probable cause	Corrective action
15. Unit will not increment when DWN key is pressed.	a. Defective DWN key.	a. Replace A1.
16. Frequency display will not flash when illegal frequency is programmed.	a. Faulty Keyboard and Display Assembly A1.	a. Replace A1.
	b. Faulty Digital Control Assembly A5.	b. Replace A5.
	c. Faulty I/O Extender A6.	c. Replace A6.
17. Unit will not display previous legal frequency when CLR key is pressed.	a. Defective CLR key.	a. Replace A1.
18. Unit will not reset to start frequency when PROGRAM/DISPLAY switch is set to START.	a. Defective switch S5.	a. Replace S5.
	b. Faulty wiring from S5 to Keyboard and Display Assembly A1.	b. Repair wiring.
	c. Faulty Keyboard and Display Assembly A1.	c. Replace A1.
19. Unit will not reset to stop frequency when PROGRAM/DISPLAY switch is set to STOP.	a. Defective switch S5.	a. Replace S5.
	b. Faulty wiring from S5 to Keyboard and Display Assembly A1.	b. Repair wiring.
	c. Faulty Keyboard and Display Assembly A1.	c. Replace A1.
20. Unit will not sweep the programmed limits.	a. Defective MODE switch S4.	a. Replace S4.
	b. Faulty wiring from S4 to Keyboard and Display Assembly A1.	b. Repair wiring.

Table 5-5. Troubleshooting Procedures-Continued

Symptom	Probable cause	Corrective action
	c. Faulty Keyboard and Display Assembly A1.	c. Replace A1.
21. Unit will not increment at selected steps.	a. Faulty INCREMENT switch S6.	a. Replace S6.
	b. Faulty wiring from S6 to Keyboard and Display Assembly A1.	b. Repair wiring.
	c. Faulty Keyboard and Display Assembly A1.	c. Repair or replace A1.
22. RF power display gives erroneous readings.	a. Defective Power Meter Assembly A3 or Power Detector A15.	a. Replace A3 and A15.
	b. Defective RF Control Assembly A4.	b. Replace A4.
	c. Faulty Digital Control Assembly A5.	c. Replace A5.
	d. Faulty I/O Extender Assembly A6.	d. Replace A6.
	e. Defective coaxial RF switch S12.	e. Replace S12.
	f. Meter not calibrated.	f. Calibrate using CAL button.
23. Output power not leveled at all frequencies.	a. Defective coaxial RF switch S12.	a. Return to depot maintenance.
	b. Defective Power Meter Assembly A3 or Power Detector A15.	b. Replace A3 and A15.
	c. Defective RF Control Assembly A4.	c. Replace A4.

Table 5-5. Troubleshooting Procedures-Continued

Symptom	Probable cause	Corrective action
24. Output power not leveled below 2 GHz.	a. Defective Switch/Pin Diode Leveler S7.	a. Replace S7.
	b. Faulty Digital Control Assembly A5.	b. Replace A5.
	c. Faulty I/O Extender Assembly A6.	c. Replace A6.
	d. Faulty RF Control Assembly A4.	d. Replace A4.
	e. Defective coaxial RF switch S12.	e. Replace S12.
	f. Defective Power Meter Assembly A3 or Power Detector A15.	f. Replace A3 and A15.
25. Output power not leveled above 2 GHz.	a. Defective Pin Leveler A14.	a. Replace A14.
	b. Faulty Digital Control Assembly A5.	b. Replace A5.
	c. Faulty I/O Extender Assembly A6.	c. Replace A6.
	d. Faulty RF Control Assembly A4.	d. Replace A4.
	e. Defective coaxial RF switch S12.	e. Return to depot maintenance
	f. Defective Power Meter Assembly A3 or Power Detector A15.	f. Replace A3 and A15.
26. Low RF output above 2 GHz.	a. Multiplier A13 out of alignment.	a. Realign A13
	b. Defective multiplier A13.	b. Replace A13.
	c. Faulty leveling loop circuitry.	c. Replace A4.
	d. Defective TWTA AR3.	d. Replace AR3.
	e. Defective Doubler/Filter Assembly A17.	e. Replace A17.

Table 5-5. Troubleshooting Procedures-Continued

Symptom	Probable cause	Corrective action
	f. Defective Doubler/Filter Assembly A16.	f. Replace A16.
	g. Defective step attenuator AT1.	g. Replace front panel assembly.
	h. Faulty connection of semi-rigid cable.	h. Locate and repair faulty cable.
27. Output excessively noisy.	a. Faulty Synthesizer Assembly A7.	a. Replace A7.
	b. Defective VCO Y1.	b. Replace Y1.
	c. Defective VCO Driver Circuit A2U1.	c. Replace Motherboard A2.
	d. Defective reference oscillator A7U20.	d. Replace A7.
	e. Faulty power supply PS1.	e. Replace PS1.
28. Spurious signals below 2 GHz.	a. Faulty Synthesizer Assembly A7.	a. Replace A7.
	b. Defective Switch/Filter Assembly A10.	b. Replace A10.
	c. Defective Switch/Filter Assembly A12.	c. Replace A12.
	d. Defective VCO Y1.	d. Replace Y1.
	e. Faulty Digital Control Assembly A5.	e. Replace A5.
	f. Faulty I/O Extender Assembly A6.	f. Replace A6.

Table 5-5. Troubleshooting Procedures-Continued

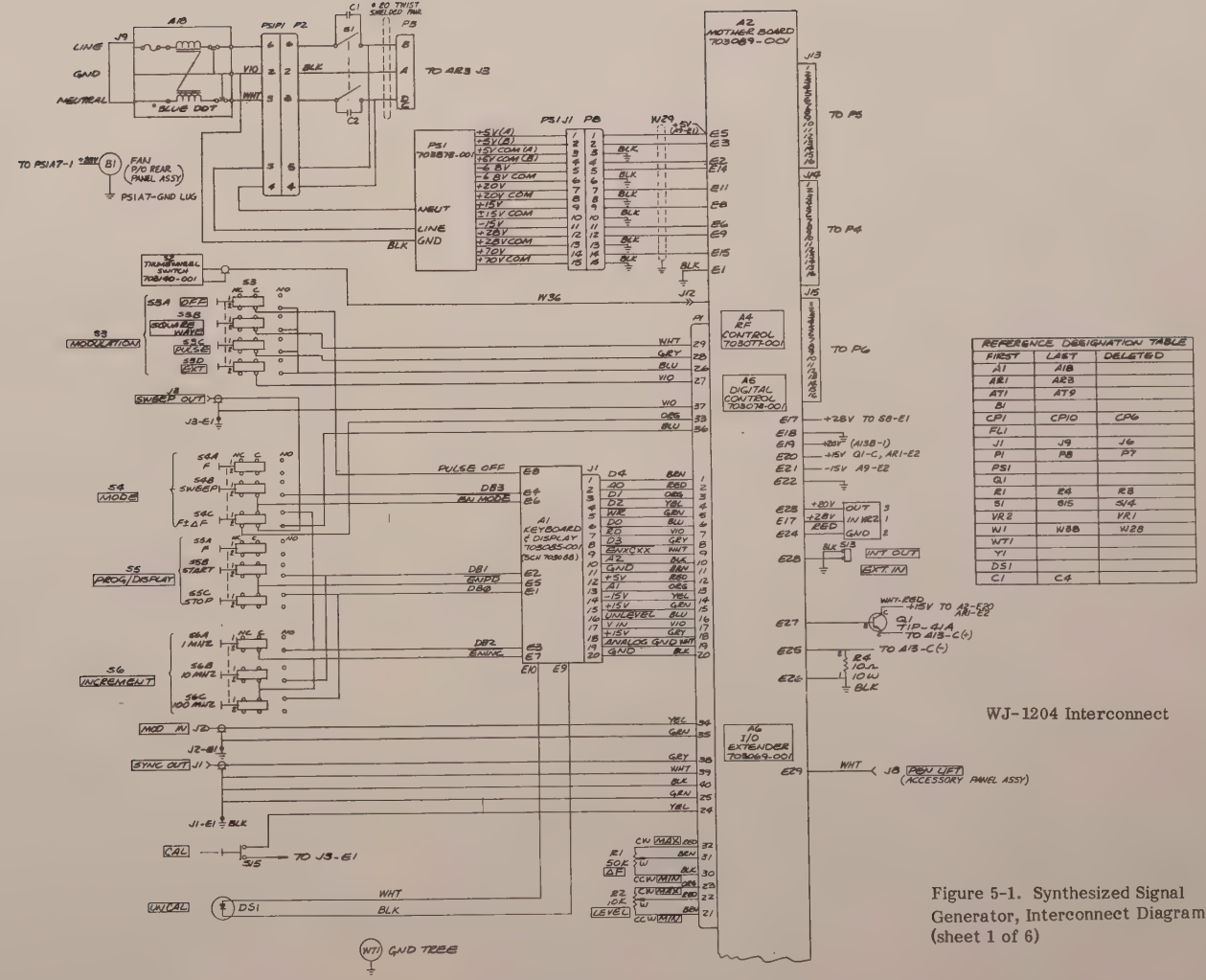
Symptom	Probable cause	Corrective action
29. Spurious signals above 2 GHz.	a. Faulty or misaligned multiplier A13.	a. Realign or replace A13.
	b. Defective Doubler/Filter A16.	b. Replace A16.
	c. Defective Doubler/Filter A17.	c. Replace A17.
30. Output not attenuated per step attenuator setting.	a. Defective step attenuator AT1.	a. Replace AT1.
31. LEVEL potentiometer will not adjust output power.	a. Defective potentiometer R2.	b. Replace R2.
	b. Faulty Level Circuitry.	b. Replace RF control A4.
32. Output remains cw when in F±ΔF mode	a. Faulty Synthesizer Assembly A7.	a. Replace A7.
	b. Faulty RF Control Assembly A4.	b. Replace A4.
	c. Faulty I/O Extender Assembly A6.	c. Replace A6.
	d. Faulty Digital Control Assembly A5.	d. Replace A5.
	e. Defective MODE switch S4.	e. Replace S4.
33. ΔF potentiometer will not affect output when in F±ΔF mode.	a. Defective potentiometer R1.	a. Replace front panel assembly.
	b. Faulty RF Control Assembly A4.	b. Replace A4.
	c. Faulty Synthesizer Assembly A7.	c. Replace A7.
	d. Faulty wiring from front panel to Motherboard Assembly A2.	d. Locate and repair faulty wiring.

Table 5-5. Troubleshooting Procedures-Continued

Symptom	Probable cause	Corrective action
34. Some or all modulation capabilities not functional.	a. Defective Modulation Select switch S3.	a. Replace S3.
	b. Faulty wiring from switch S3 to Motherboard Assembly A2.	b. Locate and repair faulty wiring.
	c. Faulty RF Control Assembly A4.	c. Replace A4.
	d. Defective Pin Modulator A9.	d. Replace A9.
	e. Faulty power supply PS1.	e. Replace PS1.
	f. Defective cable to Pin Modulator A9.	f. Replace faulty cable.
35. Incorrect or missing pulse width when in pulse modulation mode.	a. Defective thumbwheel switch S2.	a. Replace front panel assembly.
	b. Defective Modulation Select switch S3.	b. Replace front panel assembly.
	c. Faulty wiring from switch S3 to Motherboard Assembly A2.	c. Locate and repair faulty wiring.
	d. Faulty RF Control Assembly A4.	d. Replace A4.
	e. Defective Pin Modulator A9.	e. Replace A9.
36. No 5 MHz signal at rear panel BNC connection.	a. Faulty Synthesizer Assembly A7.	a. Replace A7.
	b. Defective 5 MHz reference select switch S13.	b. Replace S13.
	c. Defective cabling.	c. Locate and repair faulty cable.
	d. Faulty Digital Control Assembly A5 or I/O Extender Assembly A6.	d. Replace A5 or A6.

Table 5-6. Schematic and Power Distribution Diagrams

Figure number	Figure title
5-1	Synthesized Signal Generator, Interconnect Diagram
5-2	Keyboard and Display Circuit Card Assembly A1, Schematic Diagram
5-3	Motherboard A2, Schematic Diagram
5-4	RF Control Circuit Card Assembly A4, Schematic Diagram
5-5	Digital Control and Remote Interface Circuit Card Assembly A5, Schematic Diagram
5-6	I/O Extender Circuit Card Assembly A6, Schematic Diagram
5-7	Synthesizer Circuit Card Assembly A7, Schematic Diagram
5-8	AC Power Distribution Diagram
5-9	DC Power Distribution Diagram



REFERENCE DESIGNATION TABLE		
FIRST	LAST	DELETED
A1	A18	
AR1	AR3	
AT1	AT9	
B1		
CP1	CP10	CP6
FL1		
J1	J9	J6
P1	P8	P7
PS1		
Q1		
R1	R6	R8
S1	S15	S14
VR2		VR1
W1	W38	W28
WT1		
Y1		
DS1		
C1	C4	

WJ-1204 Interconnect

Figure 5-1. Synthesized Signal Generator, Interconnect Diagram (sheet 1 of 6)

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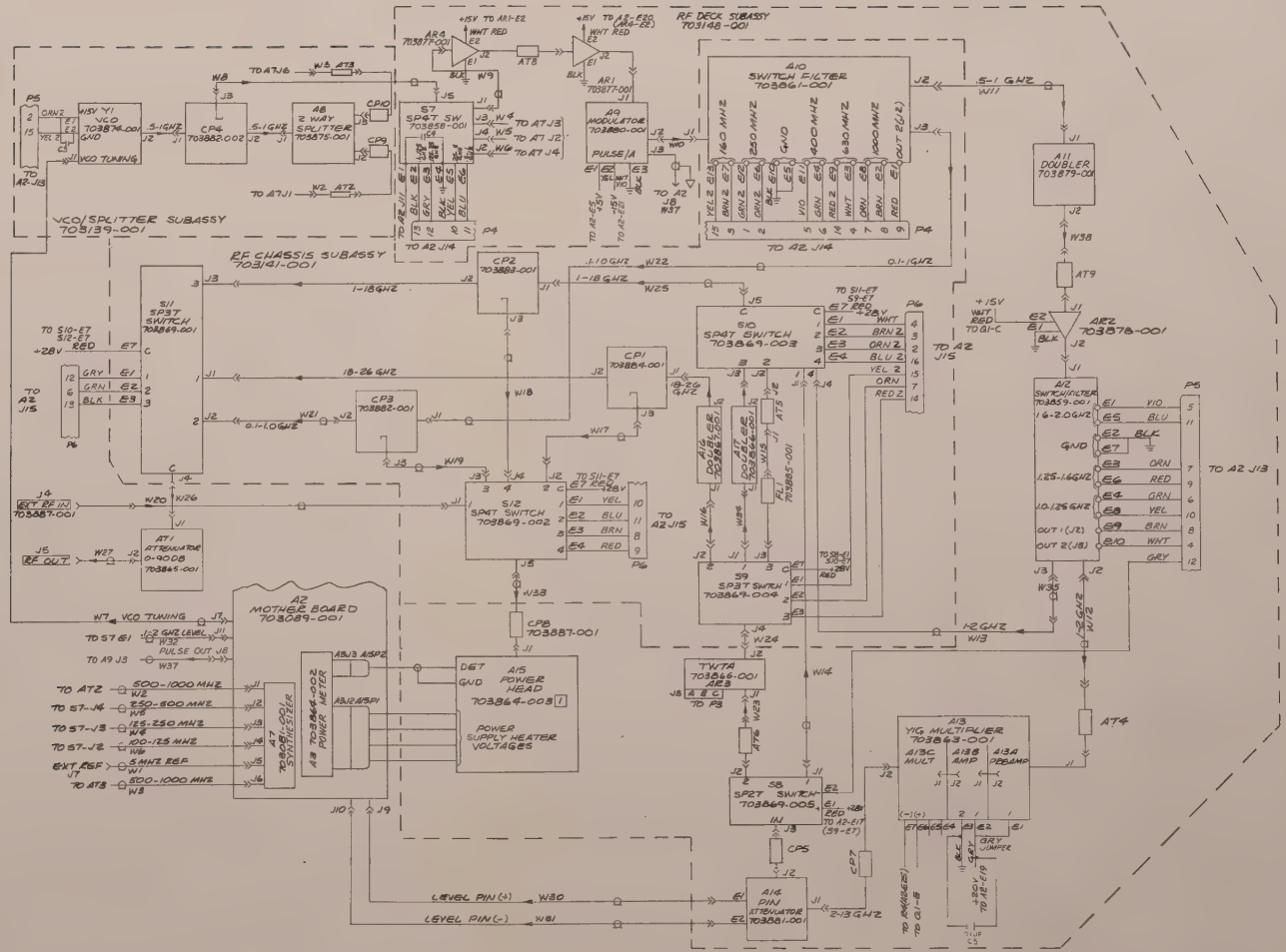


Figure 5-1. Synthesized Signal Generator, Interconnect Diagram (sheet 2 of 6)

703052C/2

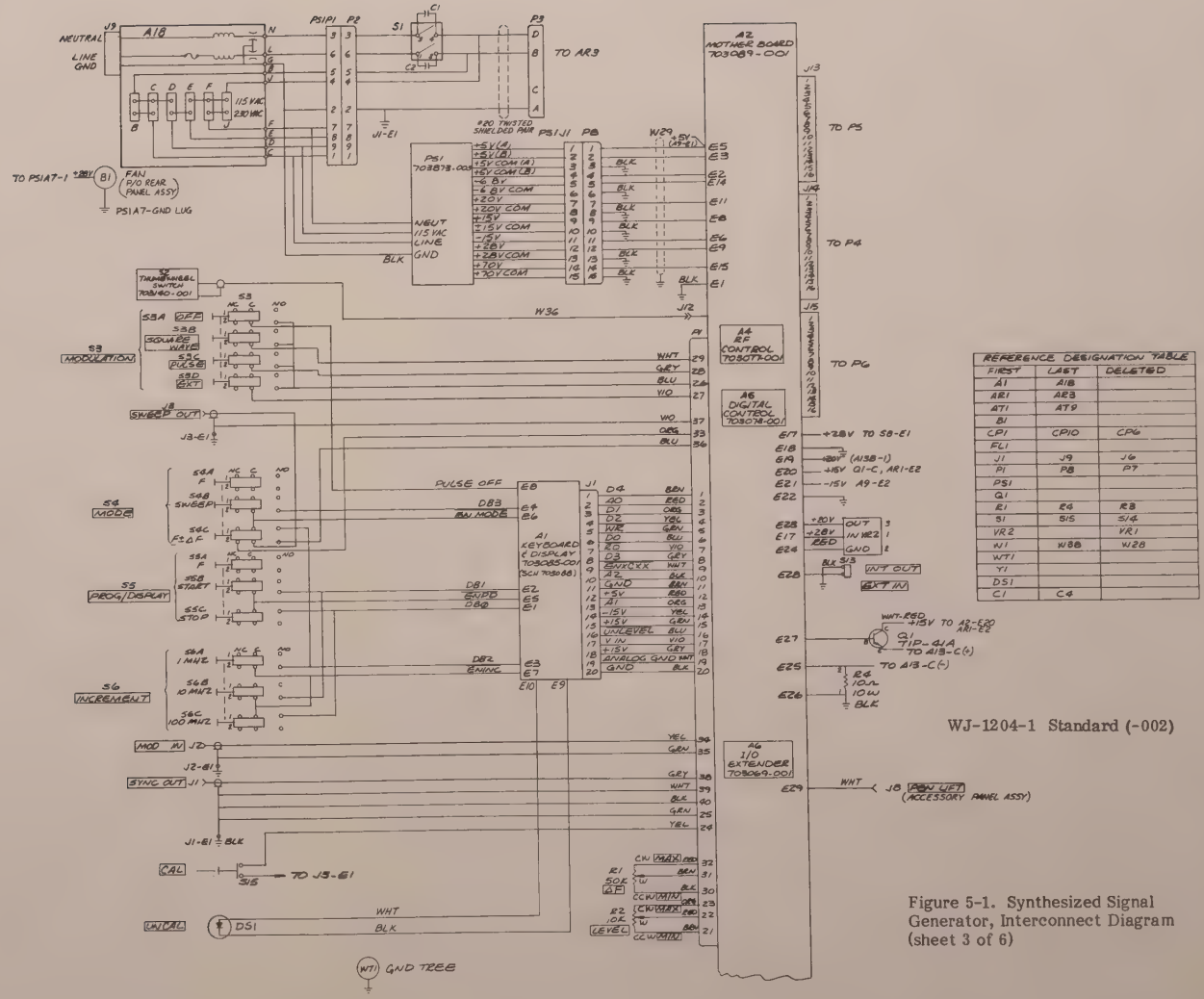
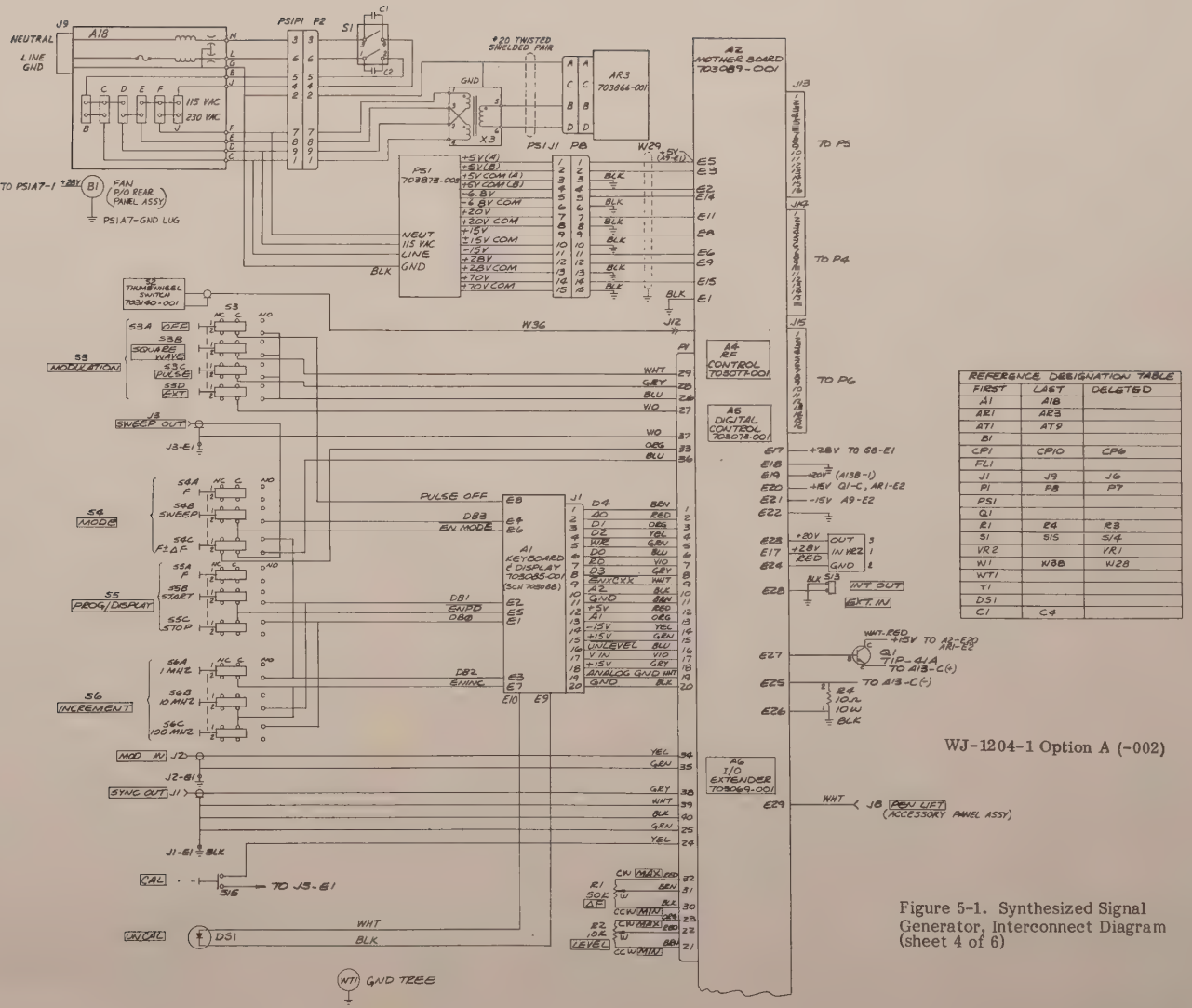


Figure 5-1. Synthesized Signal Generator, Interconnect Diagram (sheet 3 of 6)

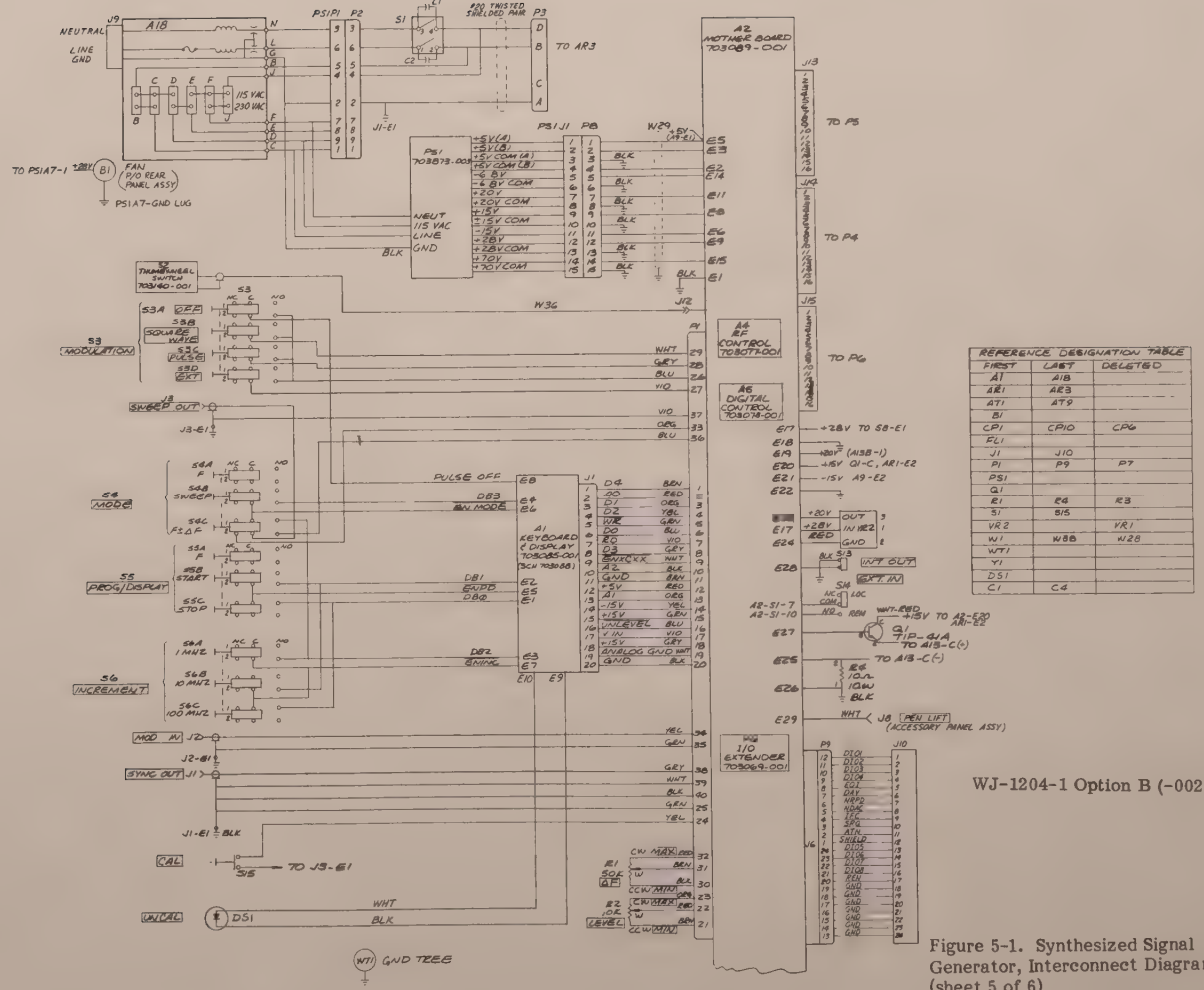
703052C/3



REFERENCE DESIGNATION TABLE		
FIRST	LAST	DELETED
A1	A18	
AR1	AR3	
AT1	AT9	
B1		
CP1	CP10	CP6
FL1		
J1	J9	J6
P1	P8	P7
PS1		
Q1		
R1	R4	R3
S1	S15	S14
VR2		VR1
W1	W38	W28
WT1		
Y1		
DS1		
C1	C4	

Figure 5-1. Synthesized Signal Generator, Interconnect Diagram (sheet 4 of 6)

703052C/4



REFERENCE DESIGNATION TABLE		
FIRST	LAST	DELETED
A1	A18	
AR1	AR3	
AT1	AT9	
B1		
CP1	CP10	CP6
FL1		
J1	J10	
P1	P9	P7
PS1		
Q1		
R1	R4	R3
S1	S15	
VR2		VR1
W1	W38	W28
WT1		
Y1		
DS1		
C1	C4	

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Figure 5-1. Synthesized Signal Generator, Interconnect Diagram (sheet 5 of 6)

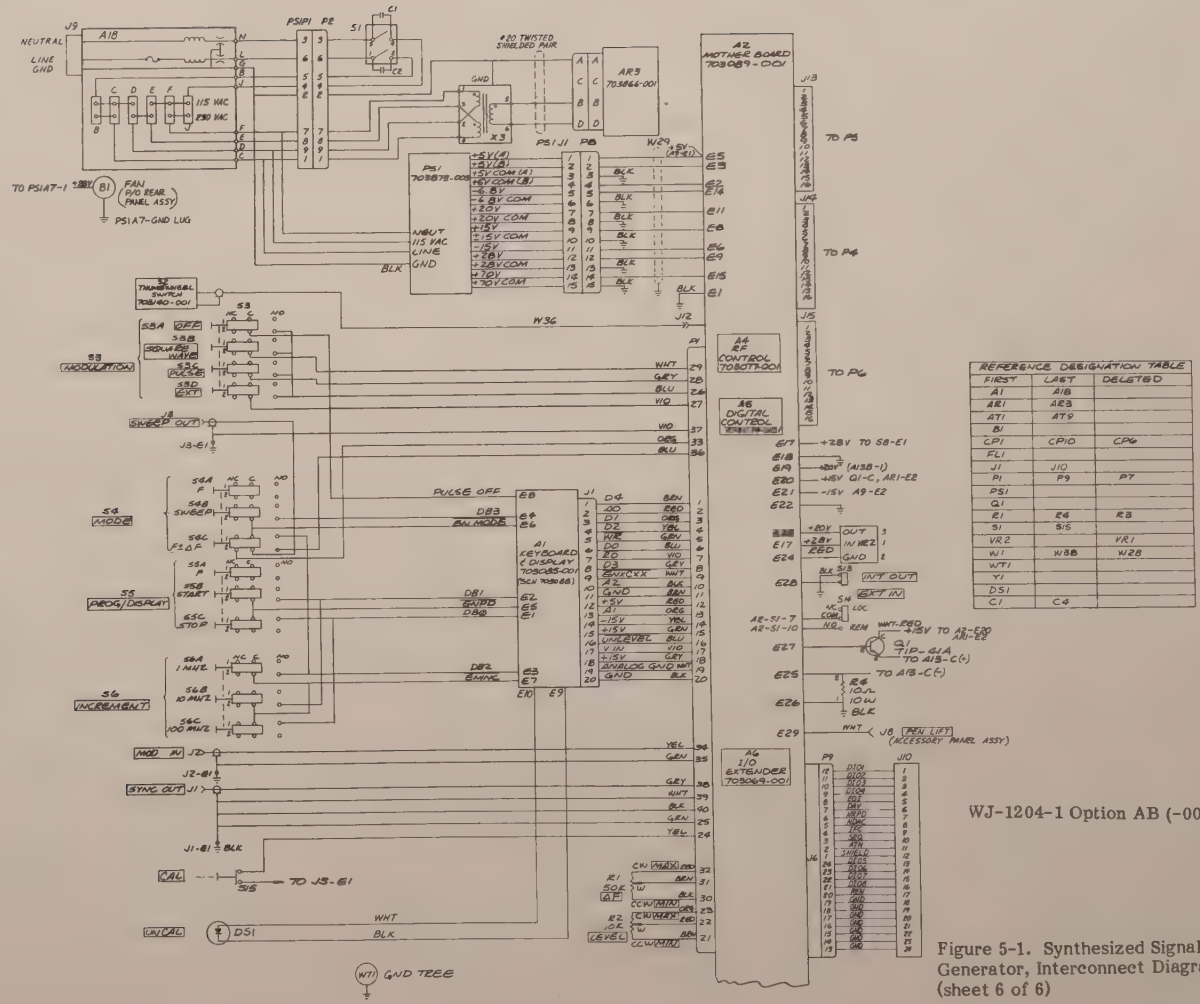
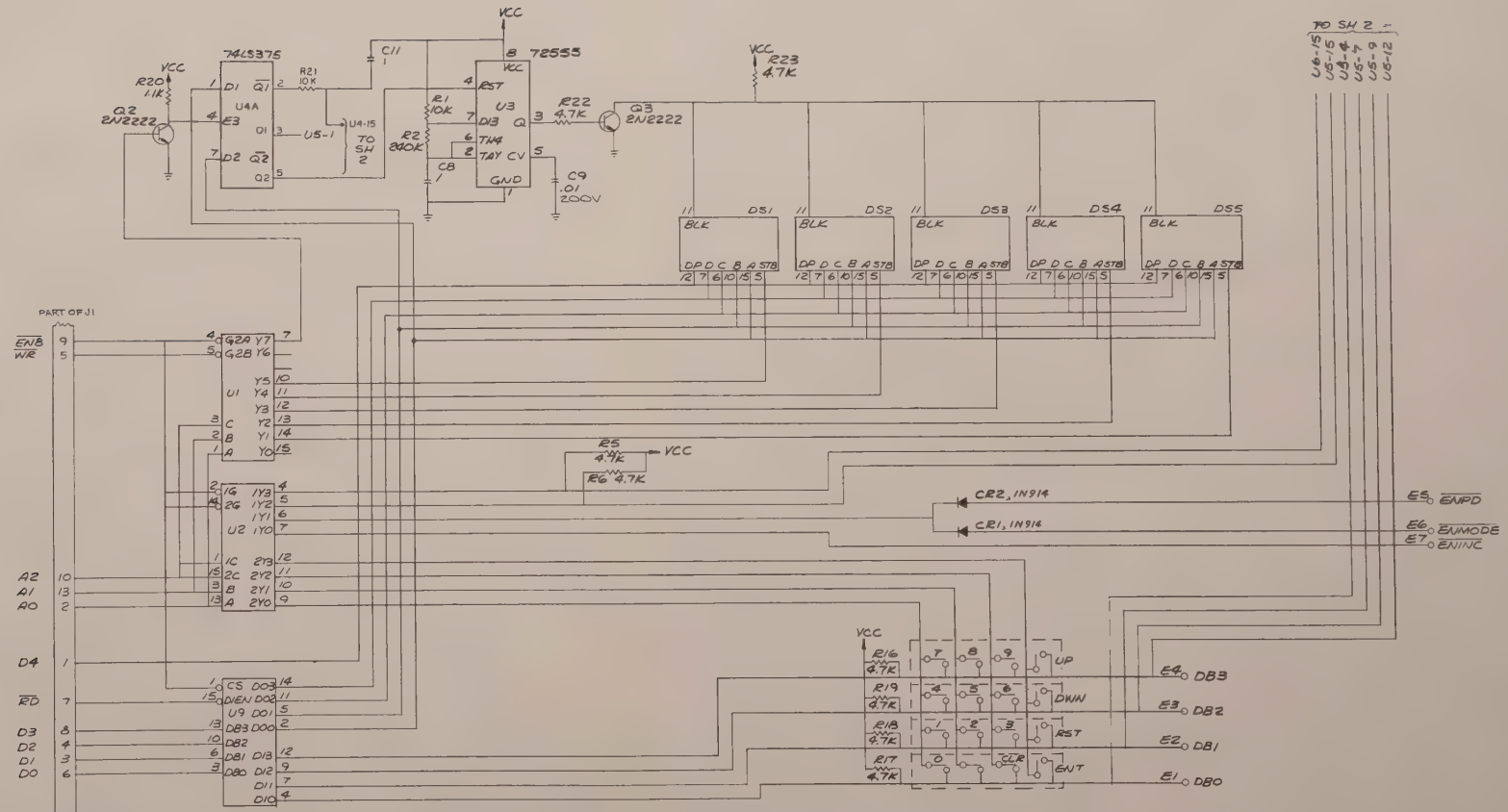


Figure 5-1. Synthesized Signal Generator, Interconnect Diagram (sheet 6 of 6)

703052C/6



COMPONENT REF DESIG		
FIRST	LAST	DELETED
R1	R25	
C1	C11	
Q1	Q3	
DS1	DS9	
U1	U9	
CR1	CR2	
VR1	VR2	
L1	L1	

INTEGRATED CIRCUIT IDENTIFICATION TABLE						
REF DESIG	TYPE	+15V	VCC	GND	-15V	CKT
U1	74LS138	–	16	8	–	1
U2	74LS156	–	16	8	–	1
U3	72555	–	8	1	–	1
U4	74LS375	–	16	8	–	2
U5, U6	74LS257	–	16	8	–	1
U7	74LS00	–	14	7	–	4
U8	LD130CJ	–	–	–	–	1
U9	8216	–	16	8	–	1
DS1-5, 7-9	TIL 308	–	16	8	–	1
DS6	TIL 304	–	14	–	–	1

1 RESISTANCE VALUES ARE IN OHMS 1/4W, 5%
CAPACITANCE VALUES ARE IN MICROFARADS, 50V, 10%

NOTES UNLESS OTHERWISE SPECIFIED

703088E/1

Figure 5-2. Keyboard and Display Circuit Card Assembly A1, Schematic Diagram (sheet 1 of 2)

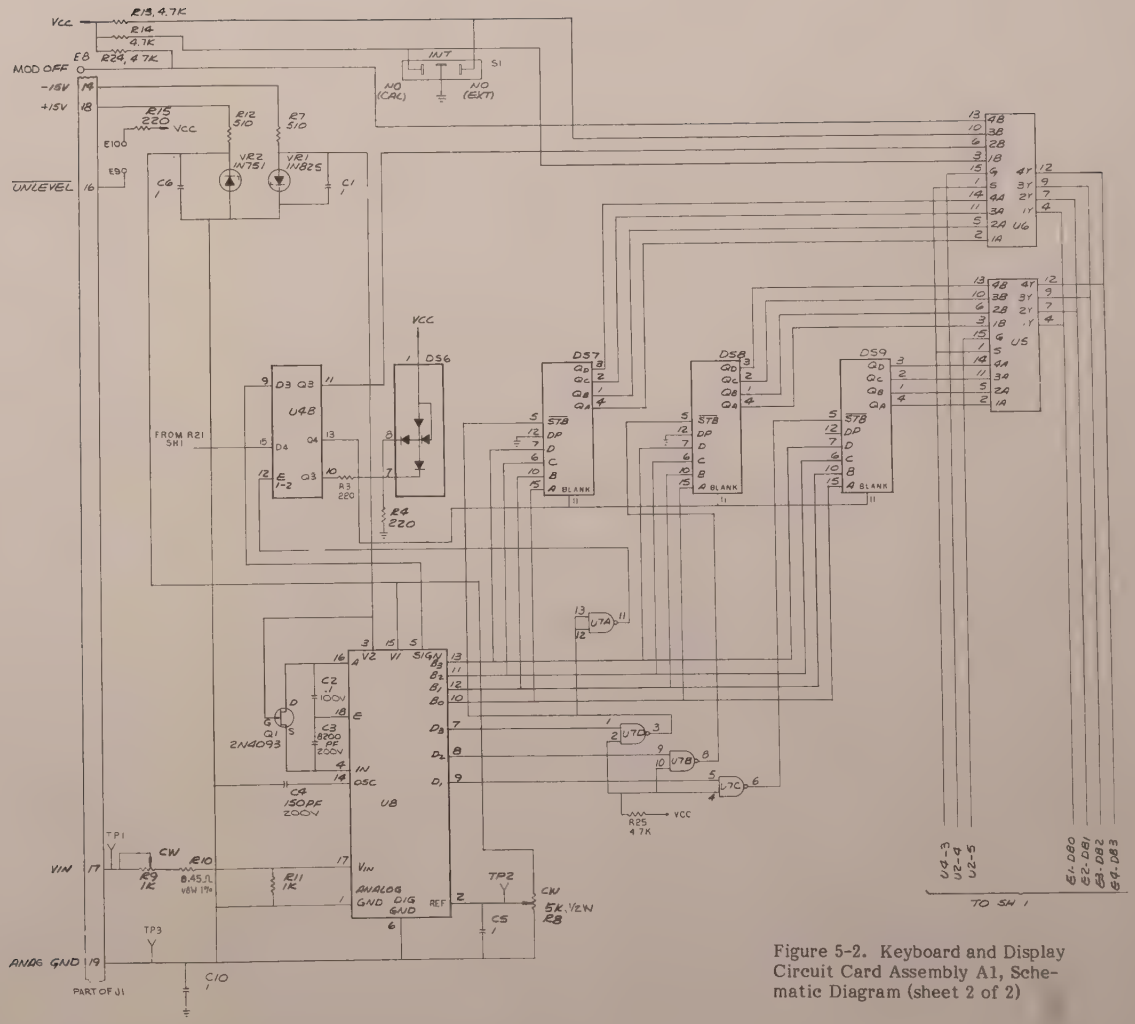


Figure 5-2. Keyboard and Display Circuit Card Assembly A1, Schematic Diagram (sheet 2 of 2)

703088E/2

Figure 5-3. Motherboard A2 Schematic Diagram (sheet 1 of 2)

703092G/1

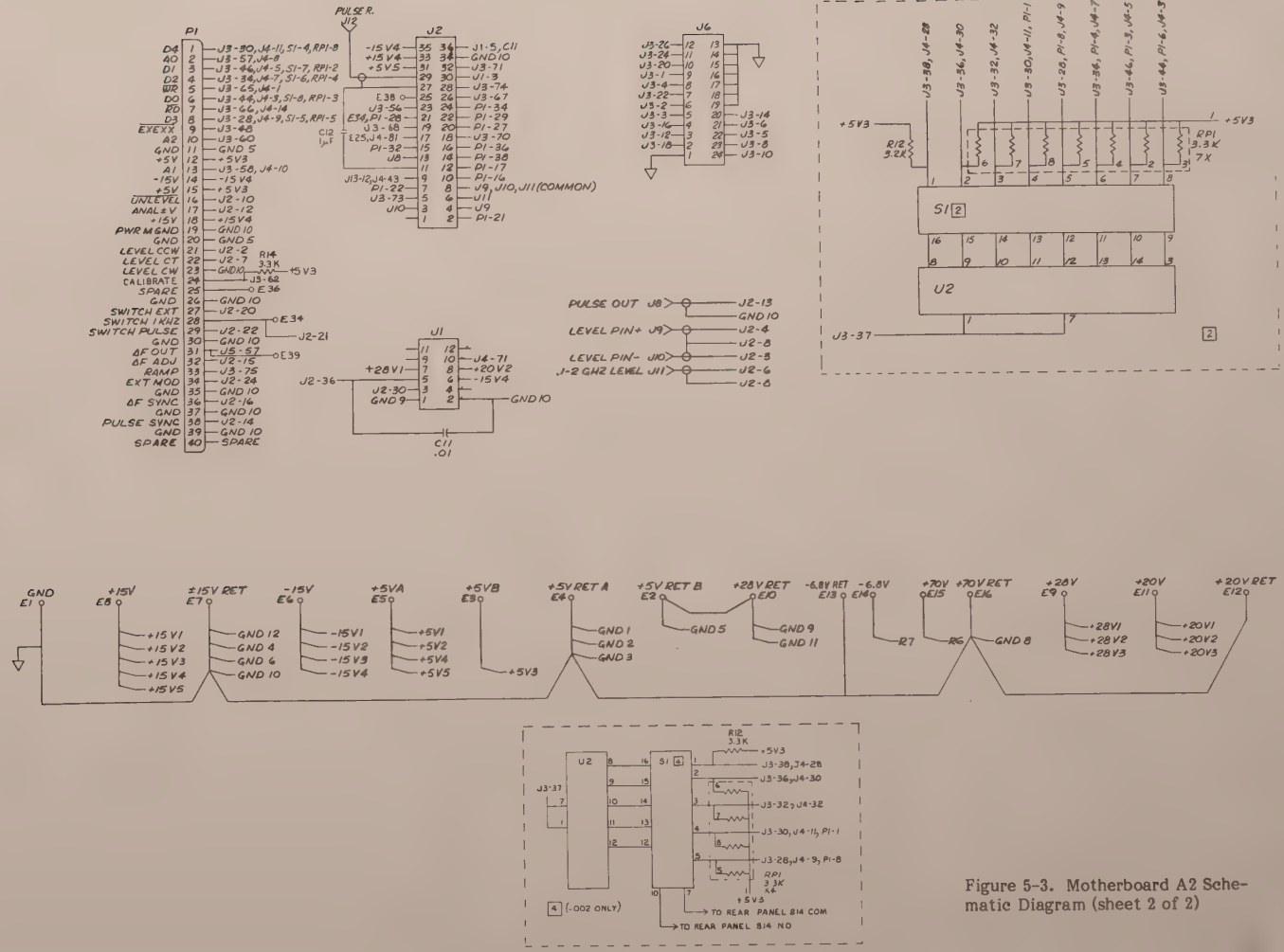


Figure 5-3. Motherboard A2 Schematic Diagram (sheet 2 of 2)

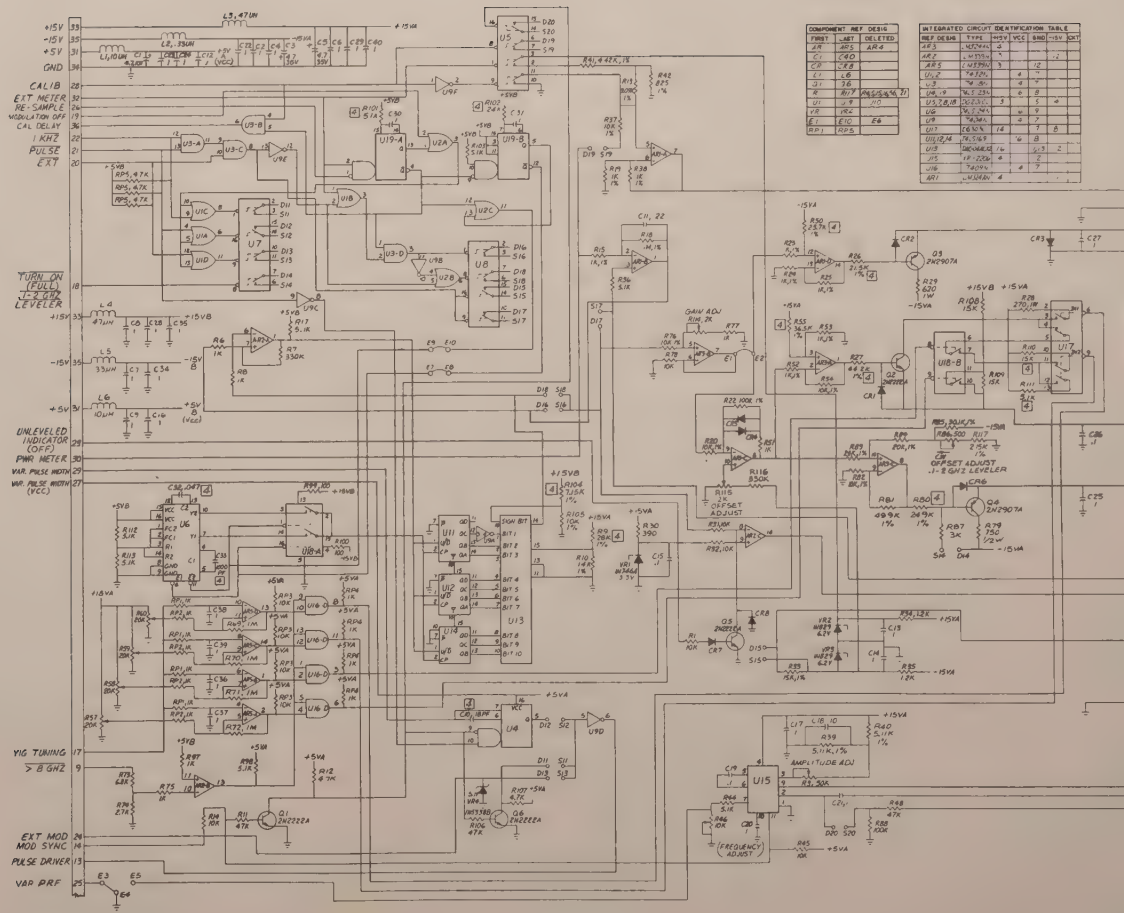
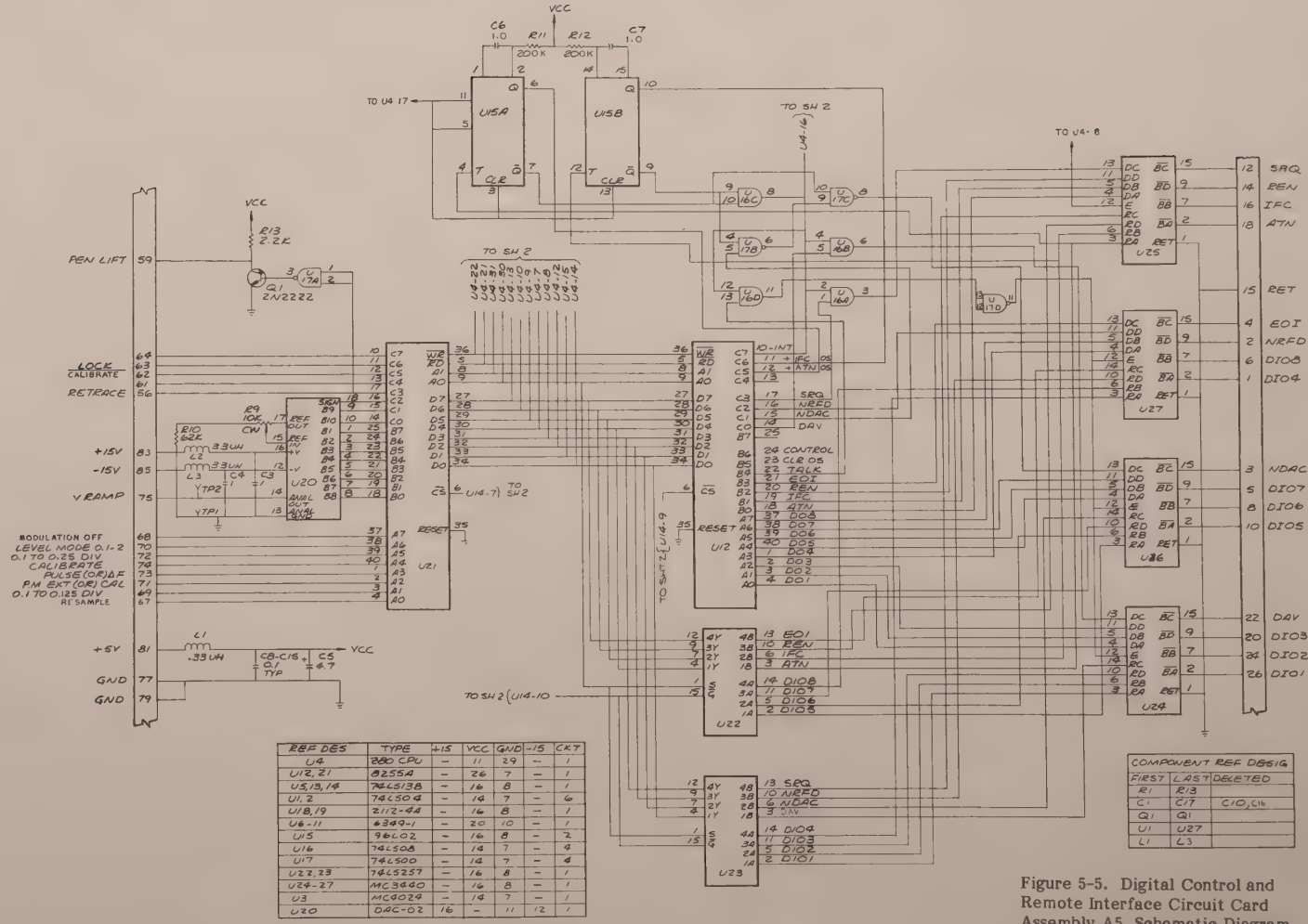


Figure 5-4. RF Control Circuit Card Assembly A4, Schematic Diagram

703080H



REF DES	TYPE	+15	VCC	GND	-15	CKT
U4	Z80 CPU	—	11	29	—	1
U12, 21	8255A	—	26	7	—	1
U5, 13, 14	74LS138	—	16	8	—	1
U1, 2	74LS04	—	14	7	—	6
U18, 19	2112-44	—	16	8	—	1
U6-11	6349-1	—	20	10	—	1
U15	96L02	—	16	8	—	2
U16	74LS08	—	14	7	—	4
U17	74L500	—	14	7	—	4
U22, 23	74LS257	—	16	8	—	1
U24-27	MC3440	—	16	8	—	1
U3	MC4024	—	14	7	—	1
U20	DAC-02	16	—	11	12	1

COMPONENT REF DESIG		
FIRST	LAST	DELETED
R1	R13	
C1	C17	C10, C16
Q1	Q1	
U1	U27	
L1	L3	

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%
CAPACITANCE VALUES ARE IN MICROFARADS.

NOTES UNLESS OTHERWISE SPECIFIED

Figure 5-5. Digital Control and Remote Interface Circuit Card Assembly A5, Schematic Diagram (sheet 1 of 2)

703076D/1

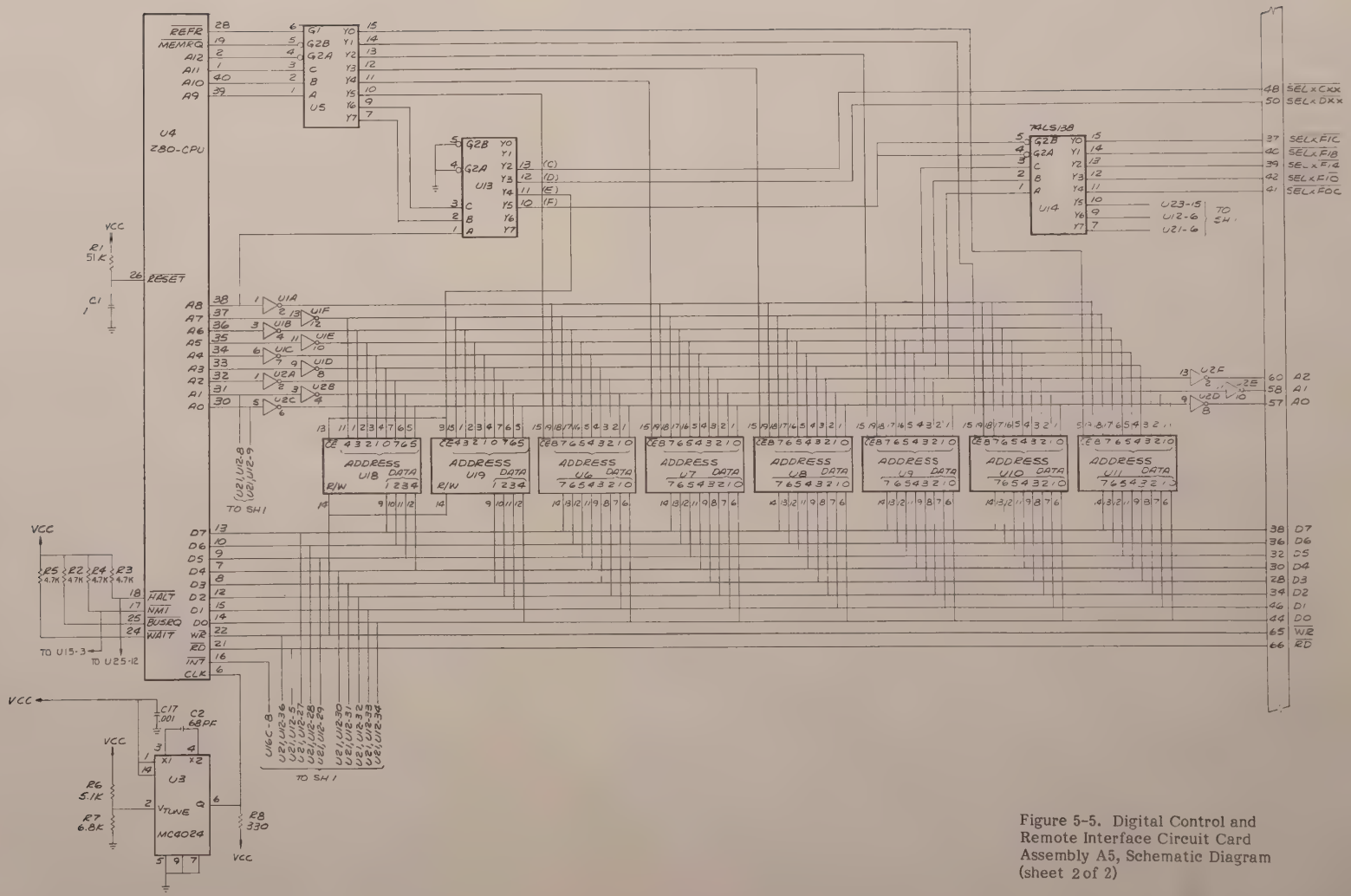


Figure 5-5. Digital Control and Remote Interface Circuit Card Assembly A5, Schematic Diagram (sheet 2 of 2)

703076D/2

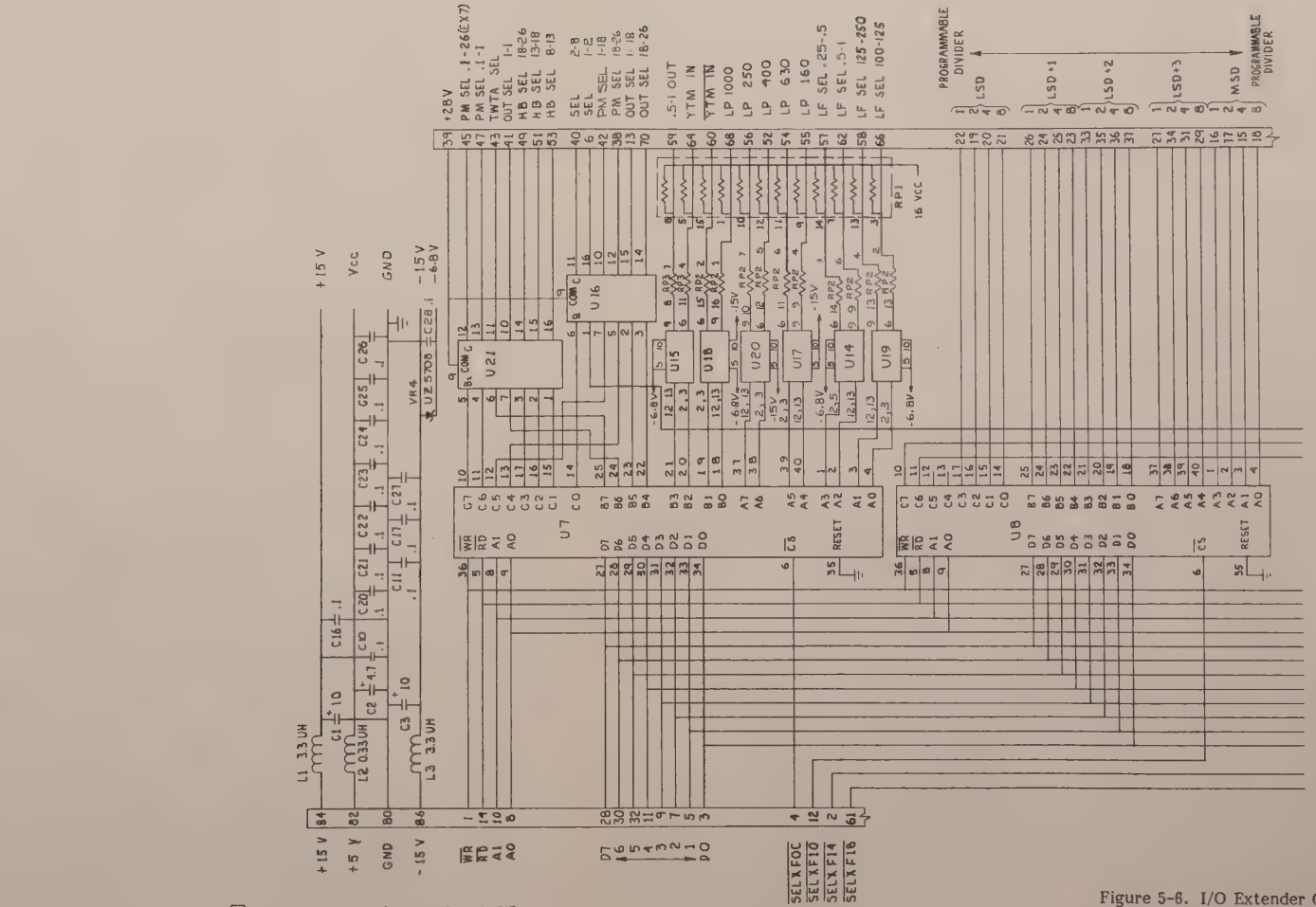
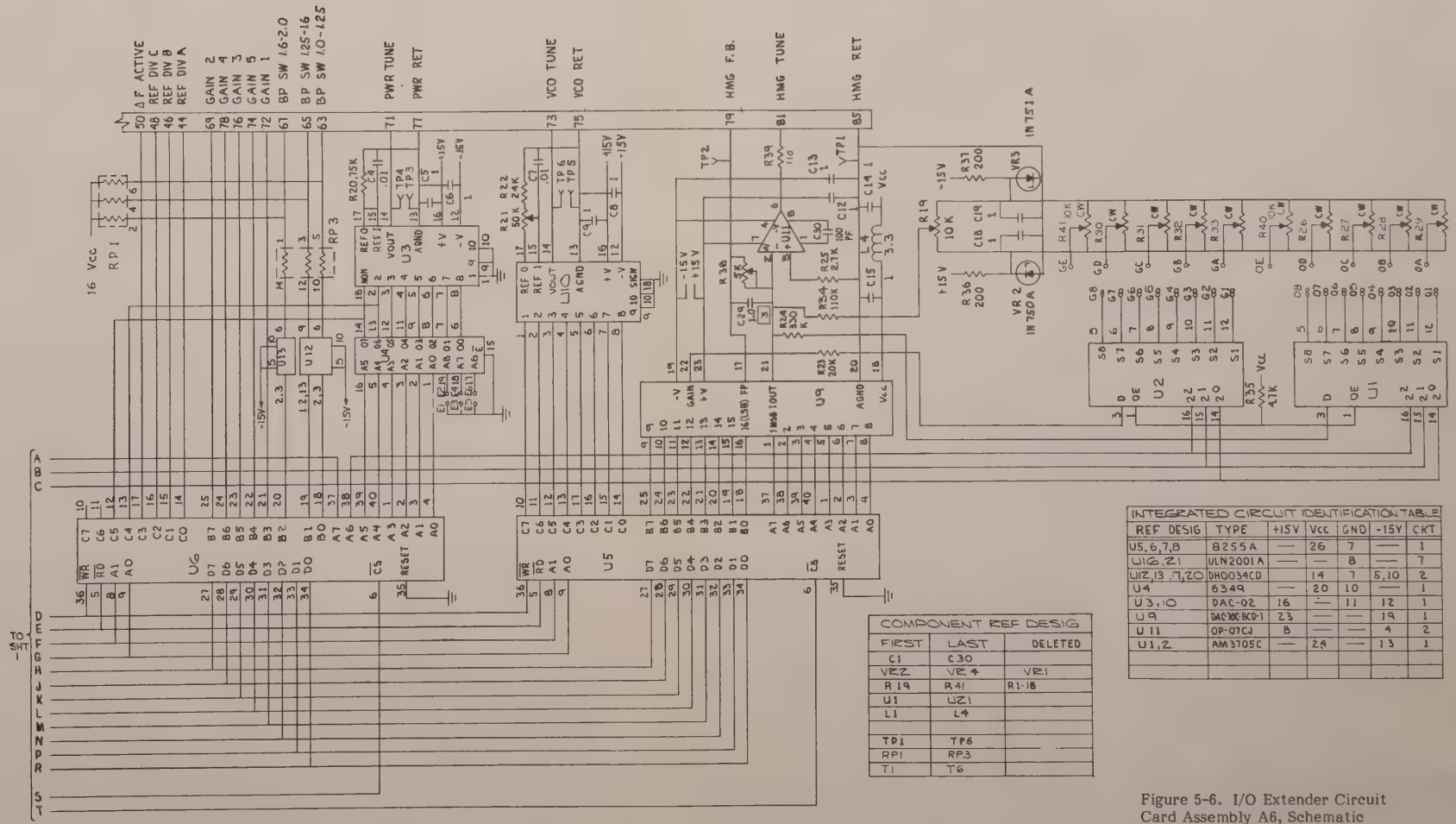


Figure 5-6. I/O Extender Circuit Card Assembly A6, Schematic Diagram (sheet 1 of 2)

703072F/1

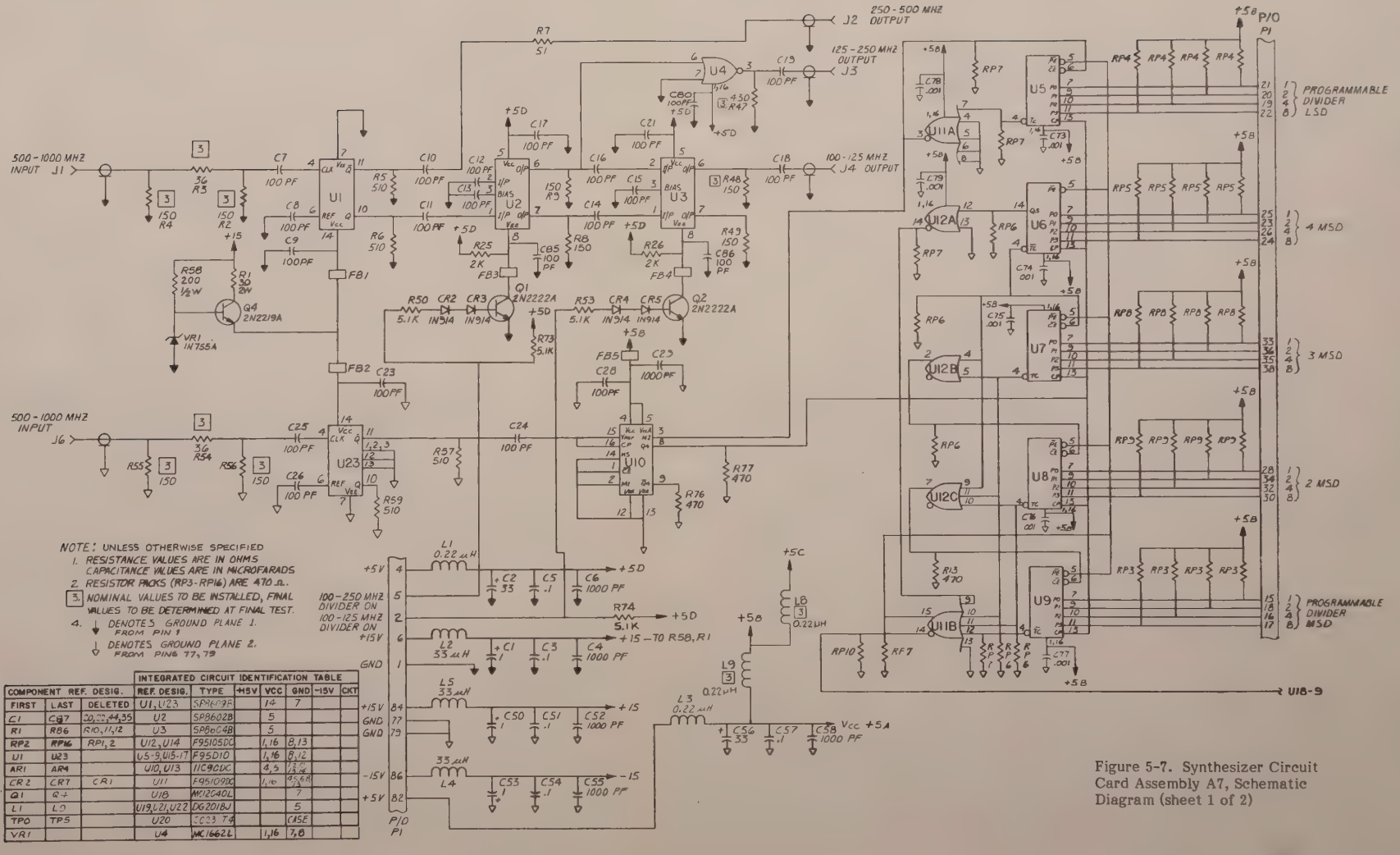


INTEGRATED CIRCUIT IDENTIFICATION TABLE						
REF DESIG	TYPE	+15V	Vcc	GND	-15V	CKT
U5,6,7,8	B255A	—	26	7	—	1
U16,21	ULN2001A	—	—	8	—	7
U12,13,17,20	DH0034CD		14	7	5,10	2
U4	6349	—	20	10	—	1
U3,10	DAC-02	16	—	11	12	1
U9	DAC10C-BCD-1	23	—	—	19	1
U11	OP-07CJ	8	—	—	4	2
U1,2	AM3705C	—	24	—	13	1

COMPONENT REF DESIG		
FIRST	LAST	DELETED
C1	C30	
VR2	VR4	VR1
R19	R41	R1-18
U1	U21	
L1	L4	
TP1	TP6	
RP1	RP3	
T1	T6	

Figure 5-6. I/O Extender Circuit Card Assembly A6, Schematic Diagram (sheet 2 of 2)

703072F/2



COMPONENT REF. DESIG.			INTEGRATED CIRCUIT IDENTIFICATION TABLE						
FIRST	LAST	DELETED	REF. DESIG.	TYPE	+5V	VCC	GND	-15V	CKT
C1	C87	20,22,34,35	U2	SP8602B		5			
R1	R86	R10,11,12	U3	SP8604B		5			
RP2	RP16	RP1, 2	U12, U14	F95105DC		1,16	8,13		
U1	U23		U5-9, U15-17	F95D10		1,16	8,12		
AR1	AR4		U10, U13	11C90DC		4,5	1/3,6/8		
CR2	CR7	CR1	U11	F95109DC		1,16	4,5,6,8		
Q1	Q4		U18	MC12040L			7		
L1	L9		U19, U21, U22	DG2018J			5		
TP0	TP5		U20	2023 T4			CASE		
VR1			U4	MC1662L		1,16	7,8		

Figure 5-7. Synthesizer Circuit Card Assembly A7, Schematic Diagram (sheet 1 of 2)

703084D/1

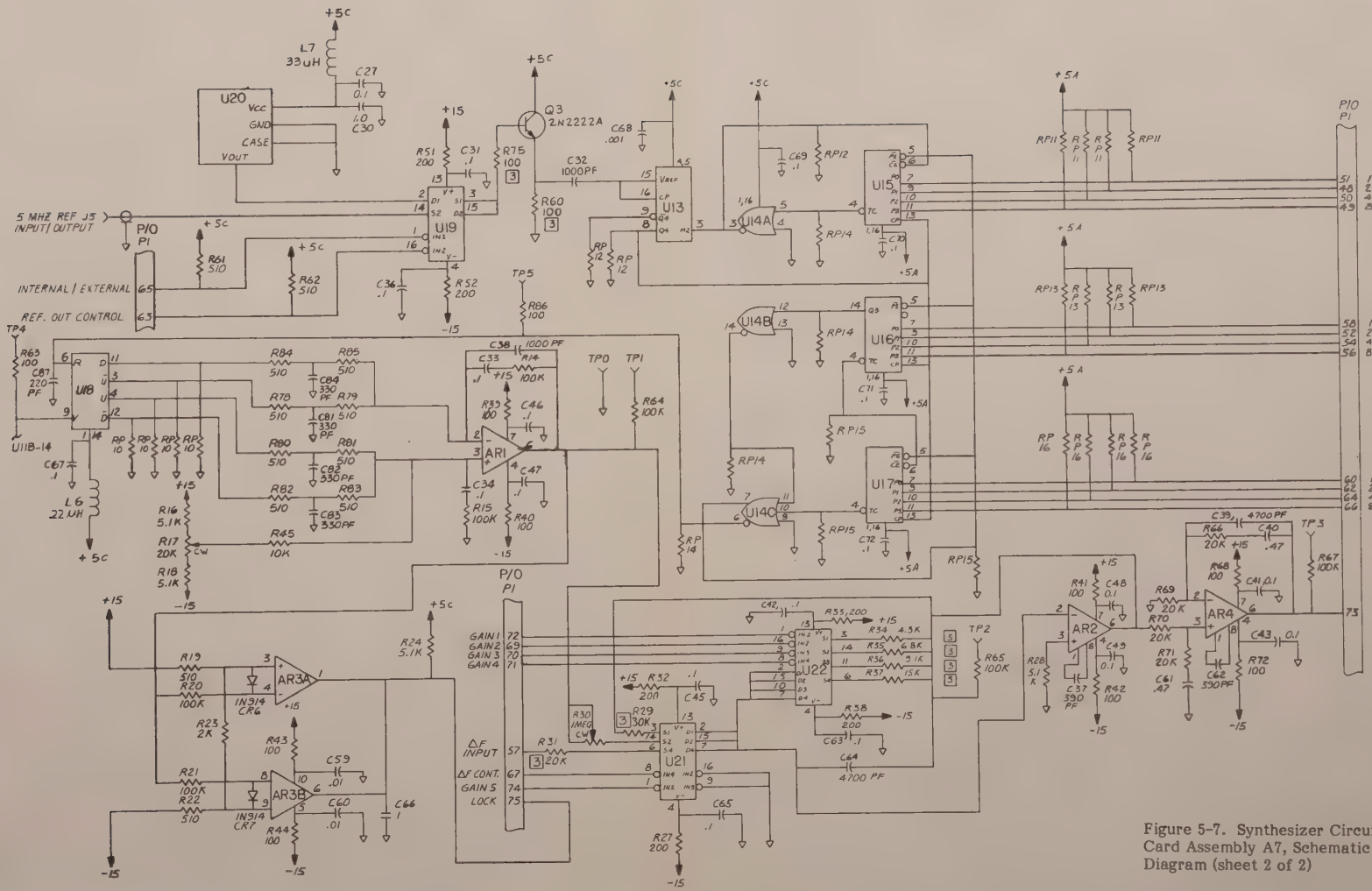


Figure 5-7. Synthesizer Circuit Card Assembly A7, Schematic Diagram (sheet 2 of 2)

703084D/2

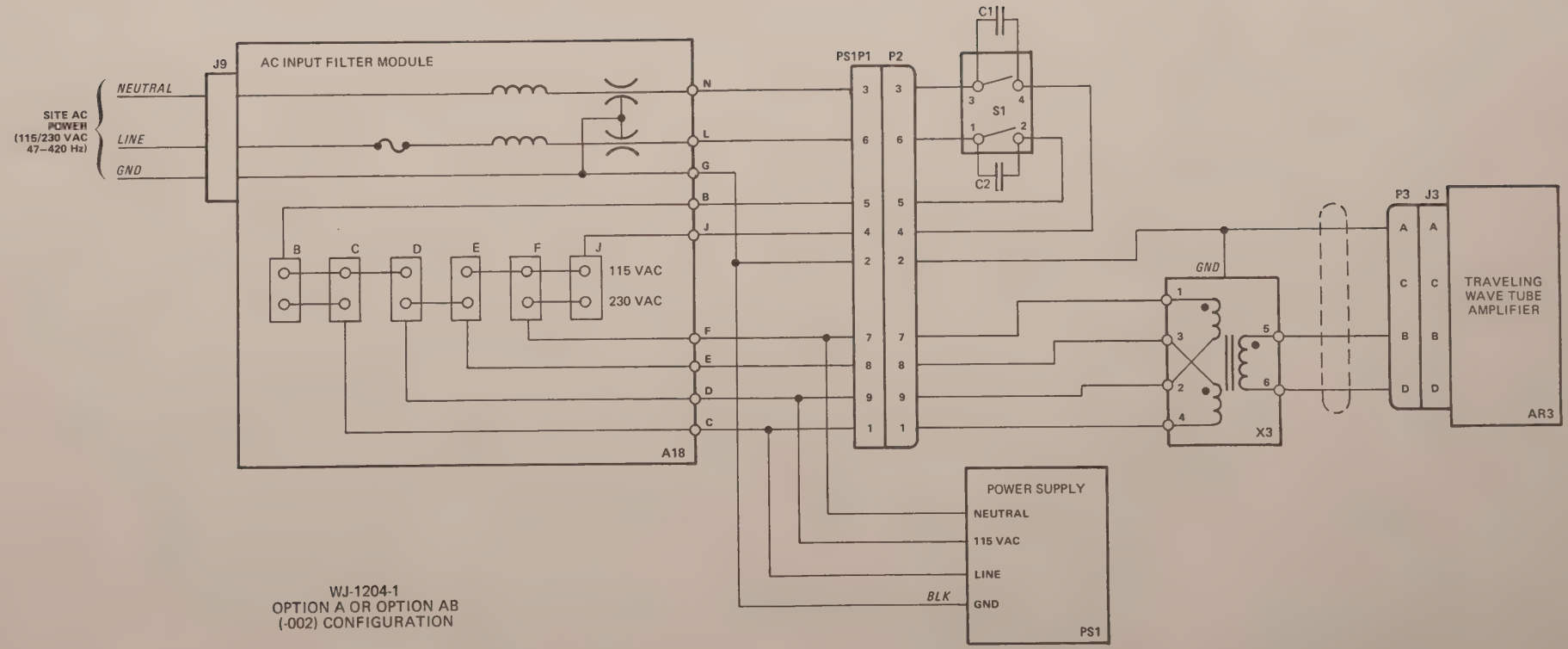


Figure 5-8. AC Power Distribution Diagram (sheet 2 of 3)

79-L-613

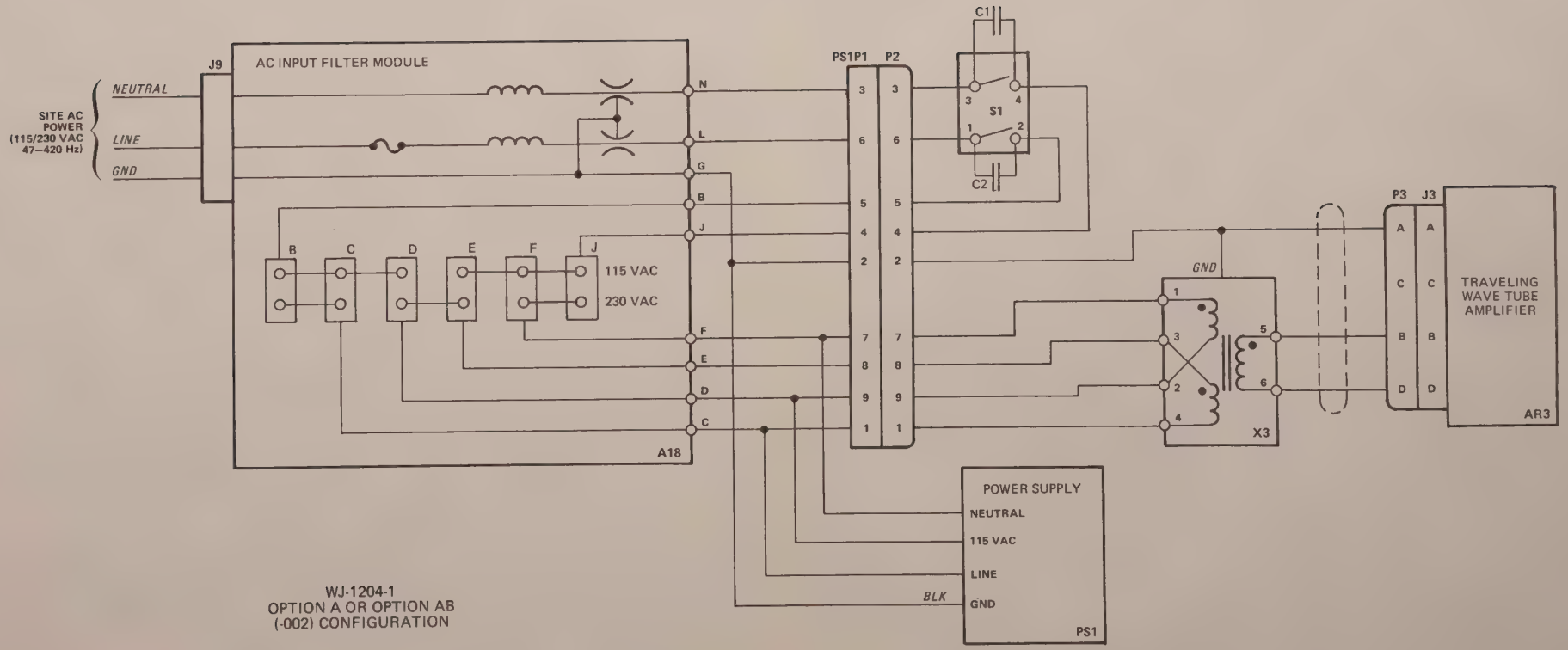


Figure 5-8. AC Power Distribution Diagram (sheet 2 of 3)

79-L-613

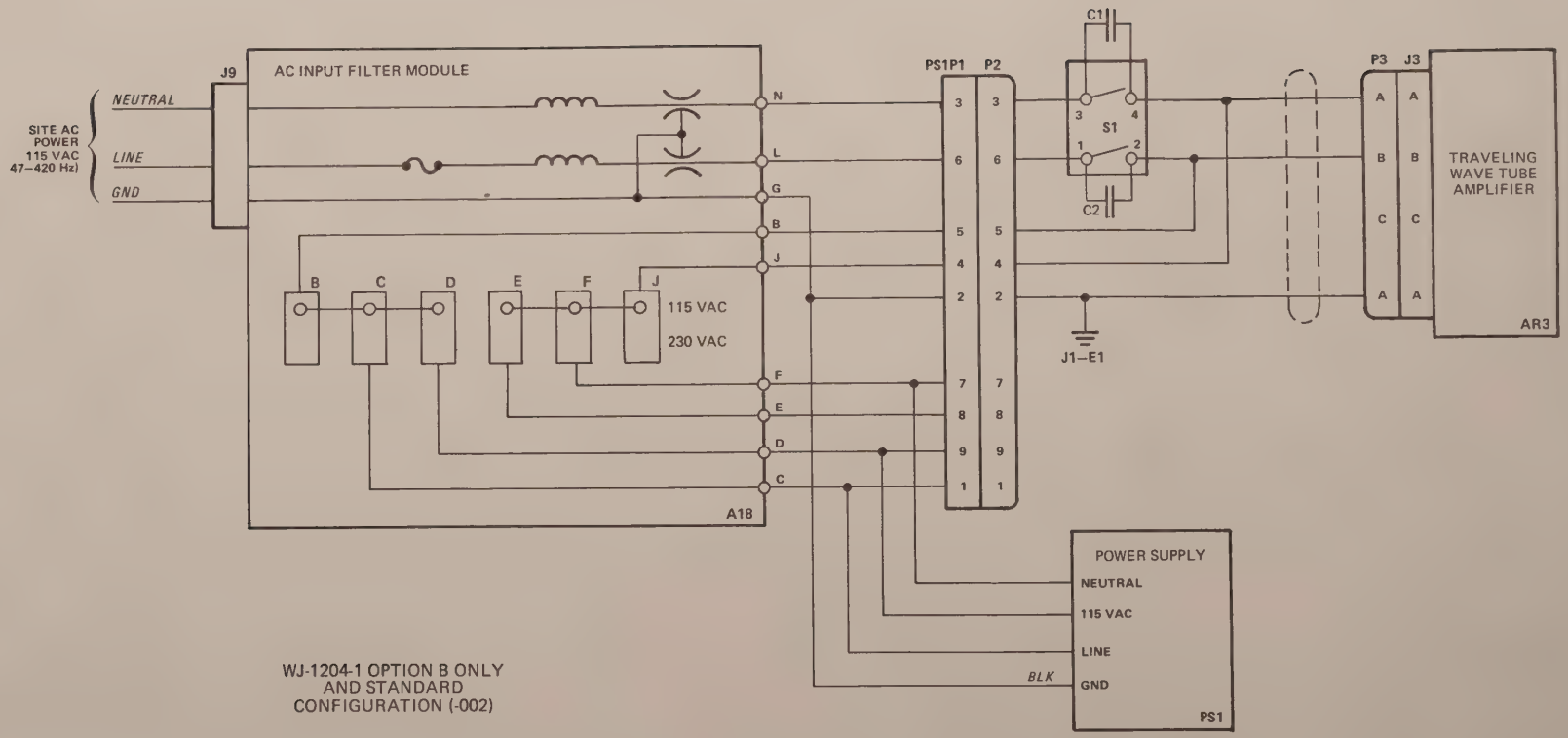


Figure 5-8. AC Power Distribution Diagram (sheet 3 of 3)

79-L-614

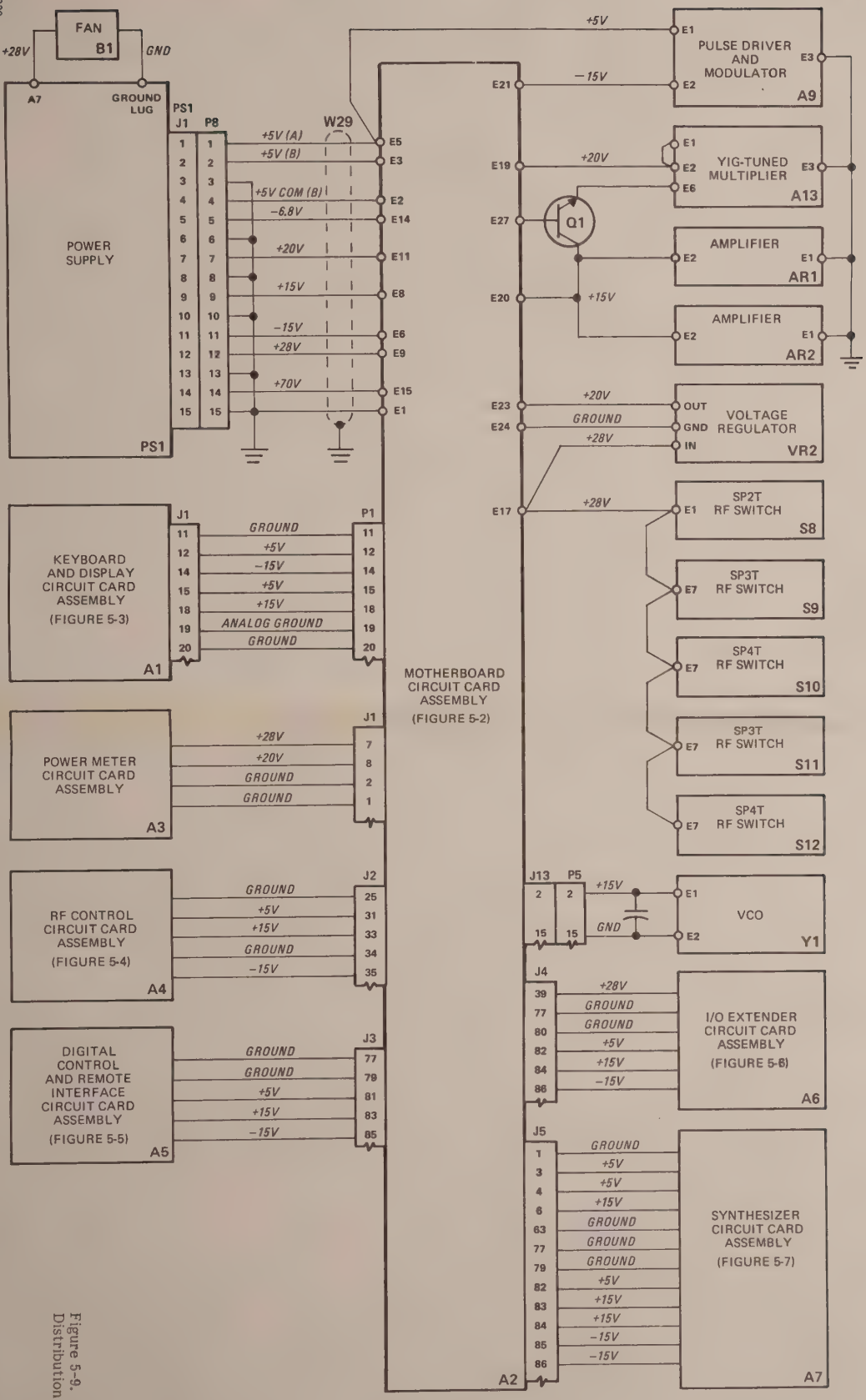


Figure 5-9. DC Power Distribution Diagram

CHAPTER 6

CORRECTIVE MAINTENANCE

6-1. INTRODUCTION. This chapter contains corrective maintenance procedures for the WJ-1204-1 Synthesized Signal Generator. Section I of this chapter consists of adjustment and alignment procedures, and section II consists of repair procedures. Reference to figures 6-1 and 6-2 and chapter 7 should be made for parts location information.

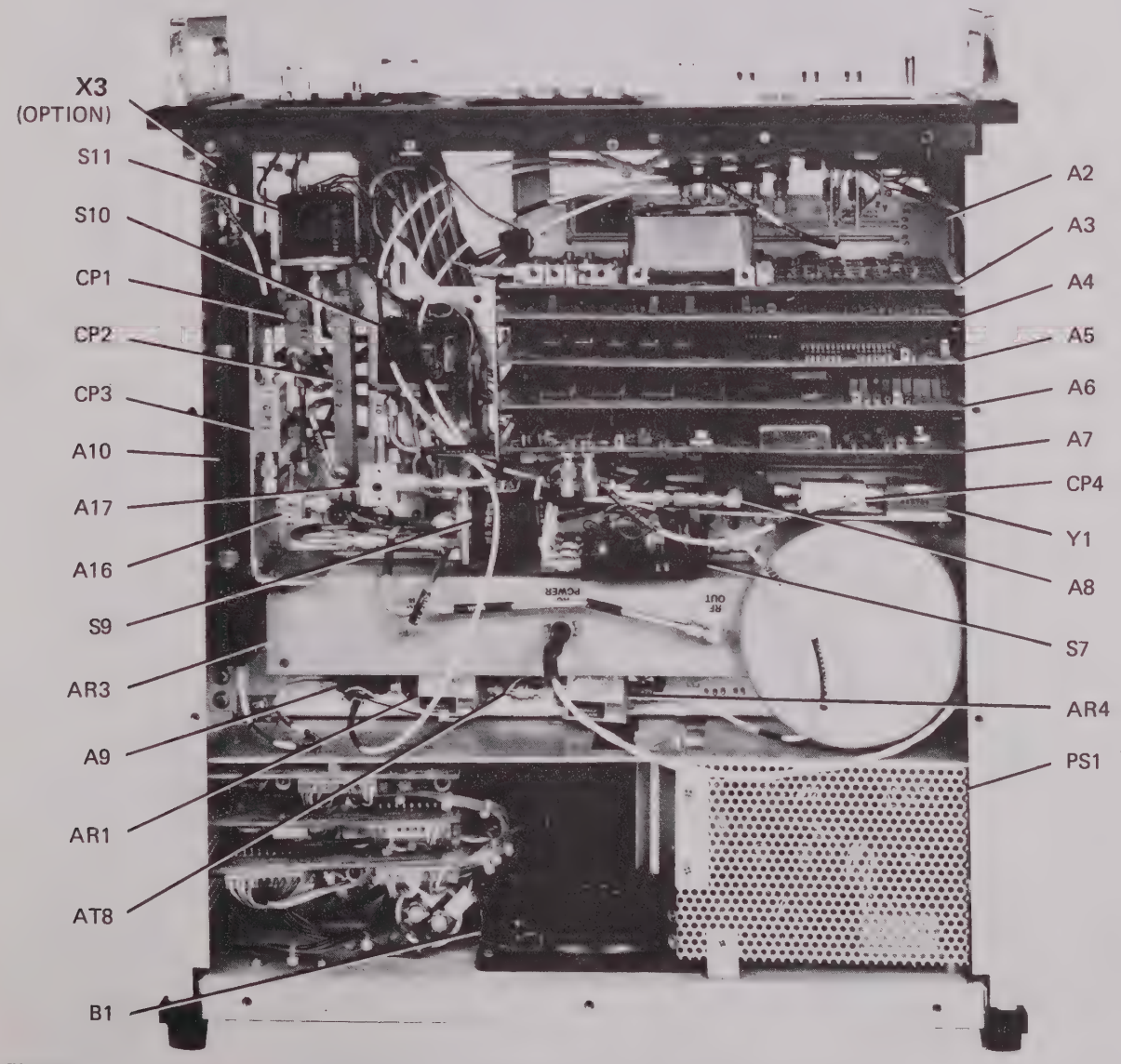
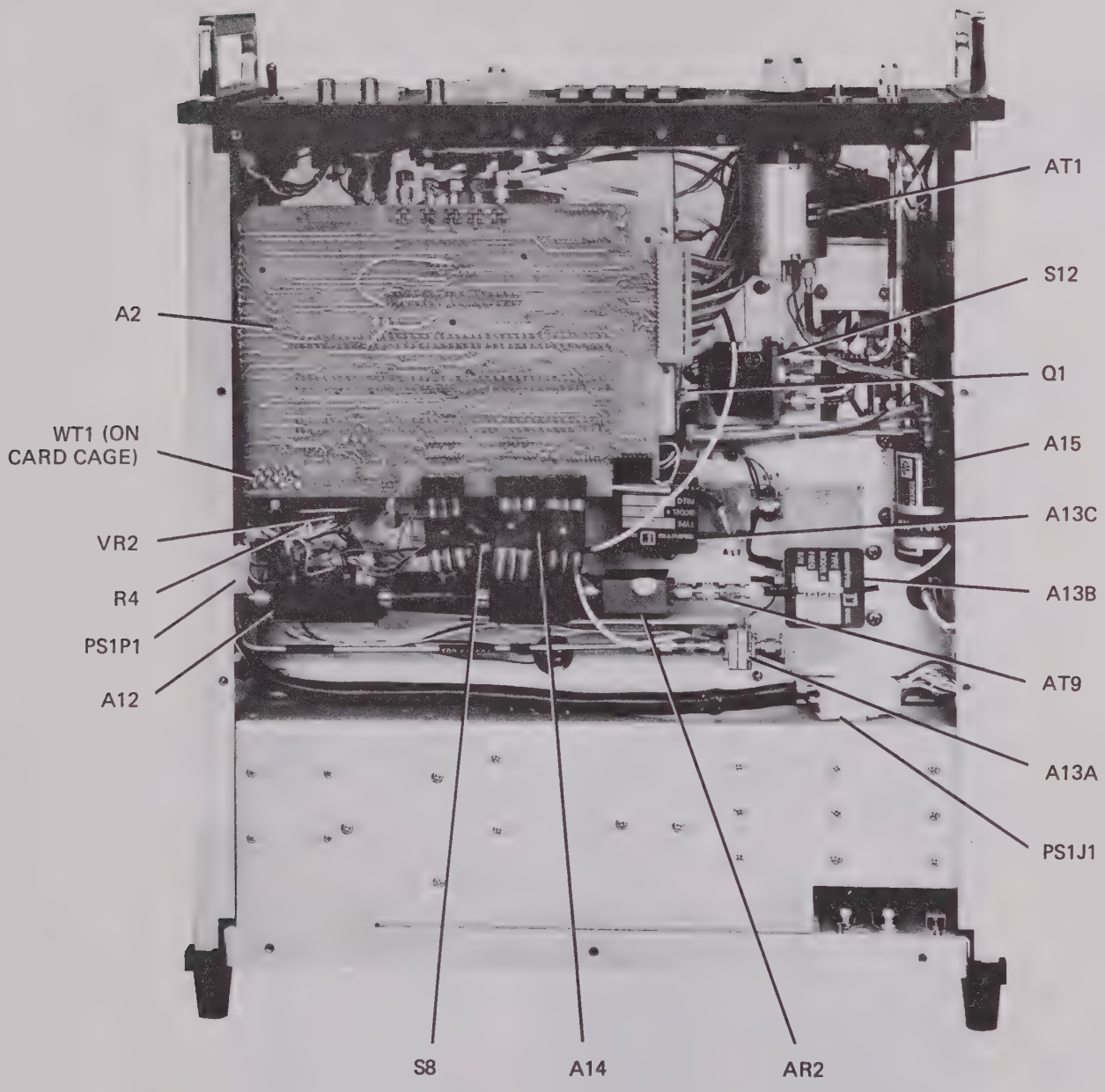


Figure 6-1. Component Locations, Top View



79-H-043

Figure 6-2. Component Locations, Bottom View

Section I. ADJUSTMENTS AND ALIGNMENTS

WARNING

Observe all safety precautions while working on the instrument.

6-2. TEST EQUIPMENT REQUIRED. Table 6-1 lists the necessary tools and test equipment for performing the adjustment and alignment procedures. Refer to table 1-3 for the required test equipment parameters.

Table 6-1. Test Equipment Required

Quantity	Nomenclature
1	Alignment tools
1	Digital multimeter
1	Frequency counter
1	Oscilloscope
1	Precision voltage source
1	Spectrum analyzer

6-3. 5 MHz REFERENCE OSCILLATOR. To align the 5 MHz reference oscillator, proceed as follows:

a. Connect a calibrated frequency counter to the rear panel 5 MHz REFERENCE connector.

b. Perform the Turn-On procedure described in table 2-3.

c. Remove the top cover by removing the cover retaining screws.

d. Using an alignment tool, turn the tuning slug of the 5 MHz oscillator (A7U20) until the counter displays 5 MHz ±5.0 Hz. (The 5 MHz oscillator is located on the Synthesizer circuit card.)

e. Reinstall the cover and return the equipment to normal operation.

6-4. VOLTAGE-CONTROLLED OSCILLATOR. To align the voltage-controlled oscillator (VCO), proceed as follows:

a. Connect a digital multimeter to A7TP3 on the Synthesizer circuit card. (Connect the ground lead to A7TP0.)

b. Mount the I/O Extender circuit card on an extender.

c. Perform the Turn-On procedure described in table 2-3.

d. Program the unit to 1.9999 GHz.

e. Adjust potentiometer A6R21 on the I/O Extender so that the voltage at A7TP3 is as close to zero volts as possible. The voltage A7TP3 should be between ±10 Vdc for a phase-locked condition.

f. Reinstall the cover and return the equipment to normal operation.

6-5. POWER METER DISPLAY. Integrated circuit A1U8 is a monolithic analog-to-digital (A/D) converter mounted on the Keyboard and Display Circuit Card Assembly. It utilizes a feedback conversion scheme to provide auto-zero and auto-polarity using a

single reference voltage. To adjust the A/D converter, proceed as follows:

a. Set POWER switch to the OFF position.

b. Remove top cover of unit.

c. Remove the RF Control Circuit Card Assembly (A4, figure 6-1). Mask off pin 12 of A4 using a small piece of non-conductive tape or other suitable material and reinstall A4 in the card file.

d. Set POWER switch to the ON position and allow a 15 minute warm-up period.

e. Connect the positive lead of a voltmeter to test point A1TP2 which is located behind the front panel.

NOTE

All test points on assembly A1 are accessible through holes drilled in the circuit card assembly.

f. Connect the negative lead of the meter to A1TP3.

g. Adjust potentiometer A1R8 until a reading of 2.000 volts is obtained. Remove the meter leads from the test points.

h. Connect the positive lead of a precision voltage source to A1TP1.

i. Connect the negative lead to A1TP3.

j. Adjust the output voltage of the source to +3.000 volts.

k. Adjust potentiometer A1R9 until the front panel power meter display reads +30.0 $\pm$ 0.1 dBm.

l. Adjust the output voltage of the source to -3.000 volts (or switch the leads of the source).

m. Verify that the power meter display reads -30.0 $\pm$ 0.1 dBm.

n. Disconnect the precision voltage source.

o. Turn off the WJ-1204-1.

p. Remove the tape from pin 12 of the RF Control Assembly. Reinstall the circuit card in the card file.

q. Reinstall the top cover.

6-6. FUNCTION GENERATOR. Integrated circuit A4U15 (figure 5-4) is a monolithic function generator which provides both a triangle wave output for the F$\pm\Delta$F function and a square wave output for the internal pulse and square wave modulation modes. The frequency of oscillation is controlled by potentiometer A4R46, and the triangle amplitude is controlled by potentiometer A4R3.

6-7. Frequency Adjustment. To adjust the output frequency of the function generator, proceed as follows:

a. Remove the top cover of the unit.

b. Connect a calibrated oscilloscope to the SYNC OUT port at the front panel.

c. Set the POWER switch to the ON position and allow a 15 minute warm-up period.

d. Press the SQUARE WAVE push-button on the front panel.

e. Observe the display on the oscilloscope and adjust A6R46 until a 1 kHz signal is obtained. This completes the adjustment procedure.

6-8. Triangle Amplitude. To adjust the amplitude of the triangle waveform, proceed as follows:

a. Remove the top cover of the unit.

b. Connect a calibrated oscilloscope to the SWEEP OUT port at the front panel.

c. Turn on the WJ-1204 and allow a 15 minute warm-up period.

d. Press the F±ΔF pushbutton switch. The ΔF sync waveform should now be observed on the oscilloscope display.

e. Adjust A4R3 clockwise until the peaks of the sync waveforms begin to flatten out. Then adjust A4R3 counterclockwise until the peaks have sharp points. This completes the adjustment procedure

6-9. SYNTHESIZER CIRCUIT CARD ASSEMBLY. The Synthesizer (A7, figure 6-1) contains two potentiometers that may need readjustment. Potentiometer A7R17 controls the bias for phase detector A7U18, and A7R30 controls the loop gain.

6-10. Phase Detector Bias. To adjust the bias of phase detector A7U18, proceed as follows:

a. Remove the top cover of the unit.

b. Turn on the unit and allow a 15 minute warm-up period.

c. Program the unit to 0.500 GHz. Press the UP button followed by the DWN button to ensure that the unit is programmed to the upper 0.5 GHz.

d. Connect an oscilloscope probe to test point A7TP1 (brown) and the ground lead to A7TP0 (black). Set the oscilloscope to ac coupled and use the most sensitive vertical scale. Set the sweep speed to 100 microseconds per division.

e. Adjust A7R17 until the amplitude of the sawtooth waveform displayed on the oscilloscope is minimum.

f. Program the unit to 0.9999 GHz and repeat steps c and e.

g. The final setting of A7R17 is a compromise of the settings obtained in steps e and f.

6-11. Loop Gain. To adjust the loop gain, proceed as follows:

a. Remove the top cover of the unit.

b. Turn on the unit and allow a 15 minute warm-up.

c. Program the unit to 0.9999 GHz.

d. Connect a calibrated spectrum analyzer to the RF OUT port on the front panel. Set the dispersion on the analyzer to 5 MHz per division and the bandwidth to 300 kHz.

e. Adjust A7R30 clockwise until the signal on the analyzer display breaks into oscillation. Then adjust A7R30 counterclockwise until the oscillation just stops. Turn the tuning slug in A7R30 two full turns counterclockwise.

f. Decrement the frequency in 10 MHz steps by using the DWN button and verify that the signal does not oscillate at any frequency. If an oscillation occurs, repeat step e at the new frequency and then continue stepping down until 0.5000 GHz is reached.

6-12. YIG TUNED HARMONIC GENERATOR. The alignment of the YIG Tuned Harmonic Generator Assembly (A13, figure 6-1) is the most critical adjustment performed on the WJ-1204-1. The steps listed below should be followed in the exact order given to ensure maximum performance from the instrument. All measurements made during this alignment must be performed carefully and accurately and should be logged for future reference.

6-13. Alignment General Description. The YIG Tuned Harmonic Generator Assembly consists of a preamplifier, a 1 watt power amplifier, and a YIG Multiplier Assembly.

The YIG Multiplier Assembly consists of a step recovery diode followed by a current tunable YIG filter. Most of the circuitry required to tune the YIG filter is located on the I/O Extender Circuit Card Assembly (A6, figure 6-1). The circuit consists of a digital-to-analog converter A6U9 whose output is proportional to the programmed frequency. The current output of A6U9 is amplified by operational amplifier A6U11 which drives transistor Q1 (figure 6-1). The emitter of Q1 flows through the multiplier tuning coil and then through 10 ohm resistor R4 to ground (figure 5-1). Both Q1 and R4 are located on the RF Deck Assembly. The ungrounded end of R4 is returned to the summing junction of A6U11 through potentiometer A6R38 thus closing the feedback loop. Potentiometer A6R38 serves as the Master Gain adjustment for the alignment. A bias current is also provided by potentiometer A6R19 which functions as the Master Offset adjustment. Multiplexer A6U1 and A6U2 are controlled by the microprocessor to switch in potentiometers A6R26 through A6R33, A6R40, and A6R41. These potentiometers provide the fine tuning Gain and Offset adjustments over different frequency bands of operation. The alignment procedure consists of adjusting A6R19, A6R38, A6R26 through A6R33, A6R40, and A6R41 to obtain the most linear tuning current for the YIG filter. For each of the operating frequency bands, an Offset potentiometer is adjusted at the lower frequency limit and a Gain potentiometer is adjusted at the upper frequency limit to center the passband of the YIG filter about the desired operating frequency. For best linearity, the YIG filter is not necessarily peaked at the operating frequency, but rather the center of the 5 dB passband is found. This procedure utilizes the instrument's internal $F \pm \Delta F$ generator to obtain the midpoints of the 5 dB passband with a minimum of difficulty. Figure 6-3 represents a typical YIG filter passband. At each frequency of interest, a display similar to

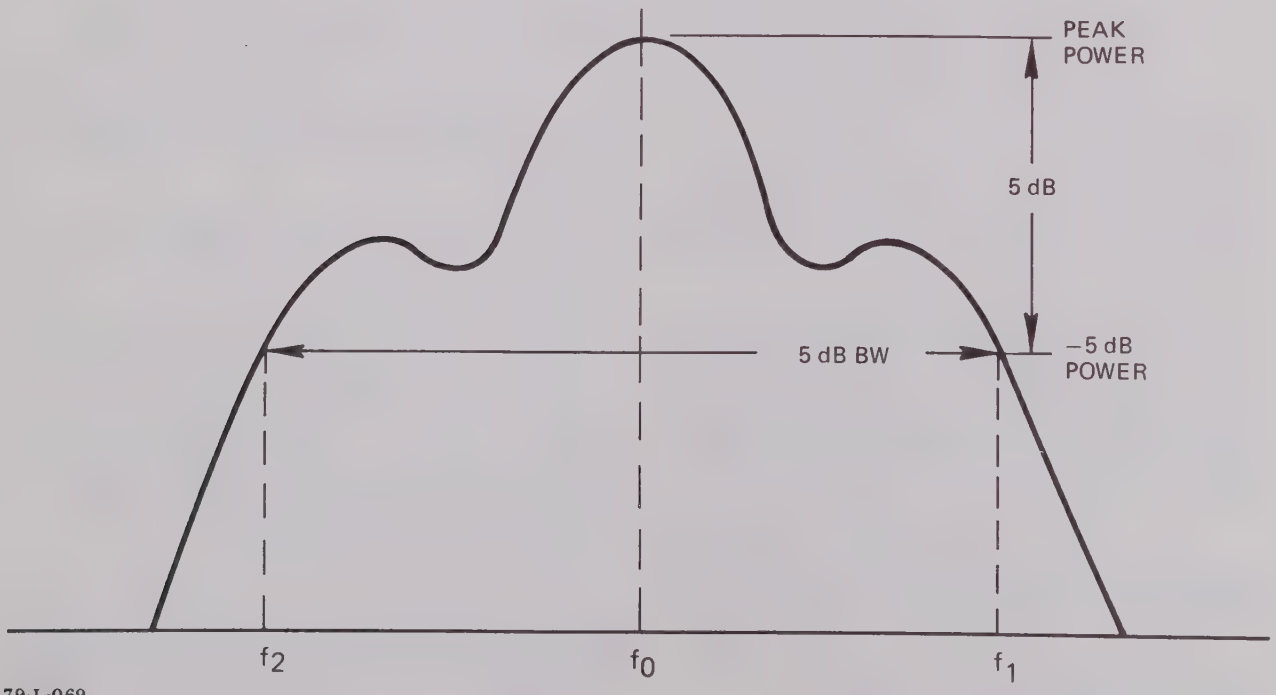


Figure 6-3. Typical YIG Filter Passband

that shown in the figure will appear on the spectrum analyzer screen, although it may be displaced to the right or to the left. The alignment procedure consists of finding the -5 dB frequencies (labeled f_1 and f_2 in the diagram) and then using one of the potentiometers to shift the display to the right or left until they are equally spaced about the analyzer's center frequency. It should be noted that this procedure may cause the filter to be tuned in a "valley" rather than on a peak as shown in the figure. Once the passband is centered on the analyzer screen, the tuning voltage may be recorded. (Tuning current is equal to the tuning voltage divided by the resistance of R4 which is 10 ohms.) This tuning voltage may then be used in place of the analyzer presentation for the iterations that follow. These iterations are necessary because the Offset and Gain potentiometers in a given frequency band interact with each other to cause a misadjustment at another band edge. Thus, the analyzer display is used once at the lower limit of each band and once at the upper limit, but is not needed thereafter.

6-14. Alignment Procedure. To align the YIG Tuned Harmonic Generator, proceed as follows:

a. Place POWER switch in OFF position and remove top and bottom covers from unit.

b. Remove CP7 and connect a calibrated spectrum analyzer to output J2 of YIG Tuned Harmonic Generator A13C (figure 7-1).

c. Remove the I/O Extender CCA (A6, figure 6-1) and mount it on an extender board. (This step is helpful but not necessary.)

d. Turn on the unit and allow a 15 minute warm-up period.

NOTE

This alignment requires that the F$\pm\Delta$F generator be operating properly and that a phaselocked 1 to 2 GHz signal be present at the input of A13 when an output frequency above 2 GHz is programmed.

e. Turn potentiometers A6R26 through A6R33, A6R40, and A6R41 to the approximate center of their range. This may require measuring the voltage at the moveable center contact of each potentiometer until zero volts is obtained.

f. Connect the negative lead of a 3 1/2-digit voltmeter to test point A6TP1 and the positive lead to A6TP2 (figure 7-16).

g. Program the unit to the "upper" 2 GHz. This is accomplished by programming the unit to 2 GHz, then pressing the UP button so that the frequency increments by one step. Press the DWN button so that the display reads 2.0000 GHz. The Multiplier Assembly is now in the RF path.

h. Connect the spectrum analyzer to the RF OUT port and tune the analyzer to 2.000 GHz. Allow a resolution of 5 or 10 MHz per division (horizontal) and 5 or 10 dB per division (vertical). Set the resolution bandwidth to 300 kHz and the sweep speed to 5 or 10 milliseconds.

i. Place the unit in the F$\pm\Delta$F mode by pressing the ΔF pushbutton on the front panel. Turn the ΔF amplitude control on the front panel fully clockwise.

j. Adjust potentiometer A6R19 until the passband of the YIG filter is centered on the analyzer screen. Keeping the analyzer center frequency at 2.000 GHz, adjust A6R19 until the upper 5 dB frequency and the lower 5 dB frequency are equidistant from the center line. Record the tuning

voltage measured between A6TP1 and A6TP2.

k. Program the unit to the "lower" 13 GHz. This is accomplished by programming 13 GHz, pressing the DWN button so that the display decrements one step, then the UP button so that 13.000 GHz is displayed.

l. Tune the spectrum analyzer center frequency to 13.000 GHz.

m. Adjust A6R38 until the YIG passband is centered on the analyzer screen. It may be necessary to decrease the ΔF amplitude at this time. The total ΔF dispersion should be kept at about 50 MHz. Record the tuning voltage.

n. Alternately program between the upper 2 GHz and the lower 13 GHz, adjusting A6R19 and A6R38 respectively until the tuning voltages measured at both limits simultaneously agree with the recorded values.

o. Program the unit to 3.999 GHz.

p. Tune the spectrum analyzer to 3.999 GHz.

q. Adjust A6R30 until the YIG passband is centered on the analyzer screen. Record the tuning voltage.

r. Program the unit to the upper 2 GHz.

s. Tune the analyzer to 2.000 GHz.

t. Adjust A6R26 until the YIG passband is centered on the analyzer screen. Record the tuning voltage.

u. Repeat steps o through t ignoring the analyzer until the tuning voltages measured at both limits simultaneously agree with the recorded values.

v. Program the unit to 4 GHz.

w. Tune the analyzer to 4.000 GHz.

x. Adjust A6R27 until the YIG passband is centered on the analyzer screen. Record the tuning voltage.

y. Program the unit to 7.999 GHz.

z. Tune the spectrum analyzer to 7.999 GHz.

aa. Adjust A6R31 until the YIG passband is centered on the analyzer screen. Record the tuning voltage.

ab. Repeat steps v through aa (ignoring the analyzer) until the tuning voltages measured at both limits simultaneously agree with the recorded values.

ac. Program the unit to 8 GHz.

ad. Tune the spectrum analyzer to 8.000 GHz.

ae. Adjust A6R28 until the YIG passband is centered on the analyzer screen. Record the tuning voltage.

af. Program the unit to the lower 13 GHz.

ag. Tune the spectrum analyzer to 13 GHz.

ah. Adjust A6R32 until the YIG passband is centered on the analyzer screen. Record the tuning voltage.

ai. Repeat steps ac through ah (ignoring the analyzer) until the tuning voltages measured at both limits simultaneously agree with the recorded values.

aj. Program the unit to the upper 13 GHz.

ak. Tune the spectrum analyzer to 6.500 GHz.

al. Adjust A6R29 until the YIG passband is centered on the analyzer screen. Record the tuning voltage.

am. Program the unit to 15.999 GHz.

an. Tune the spectrum analyzer to 7.9995 GHz.

ao. Adjust A6R33 until the YIG passband is centered on the analyzer screen. Record the tuning voltage.

ap. Repeat steps aj through ao until the tuning voltages measured at both limits simultaneously agree with the recorded values.

aq. Program the unit to 8.000 GHz.

ar. Tune the spectrum analyzer to 8.000 GHz.

as. Adjust A6R40 until the YIG passband is centered on the analyzer screen. Record the tuning voltage.

at. Program the unit to 26 GHz.

au. Tune the spectrum analyzer to 13 GHz.

av. Adjust A6R41 until the YIG passband is centered on the analyzer screen. Record the tuning voltage.

aw. Repeat steps aq through av until the tuning voltages measured at both limits simultaneously agree with the recorded values.

ax. The YIG Tuned Harmonic Generator is now aligned over its full range. If the unit becomes misaligned over any of the frequency segments described above, it will only be necessary to perform the alignment for that particular segment. Potentiometers A6R19 and A6R38 will affect everything, however, and should not be readjusted if possible.

Section II. REPAIR

6-15. GENERAL. Replacement of certain subassemblies may require realignment of other circuitry. Table 6-2 lists the alignment circuitry affected and the corresponding alignment procedure for each subassembly repaired. Some repair procedures require that wires be unsoldered from the faulty part. Tag all wires before unsoldering.

CAUTION

The WJ-1204-1 is a factory calibrated instrument that requires recalibration when certain parts are replaced or removed for any reason. Do not attempt to repair the unit when any of the following assemblies require replacement or temporary removal:
couplers CP1, CP2, CP3, CP8
attenuator AT1
power meter CCA A3
power head A15
RF switches S11, S12
Front panel connector J5
cables W17, W18, W19, W21, W26, W27, W33
Return instrument to depot maintenance for recalibration of Power Meter CCA.

Table 6-2. Alignment Required After Repairs

Subassembly	Alignment circuitry	Paragraph reference
YIG Multiplier A13	I/O Extender CCA: R19, R26 through R33, R38, R40, R41	6-12
VCO Y1	Synthesizer CCA: R17, R30	6-9
	I/O Extender CCA: R21	6-4
Synthesizer CCA A7	Synthesizer CCA A7	6-3, 6-9
I/O Extender CCA A6	I/O Extender CCA A6	6-4, 6-12

6-16. REMOVAL OF COVERS. It is necessary to remove the covers to perform internal maintenance on the WJ-1204-1. The required cover may be removed by unscrewing the ten machine screws holding the cover.

CAUTION

When reinstalling the cover do not tighten the machine screws until all ten screws are on. This will prevent warping due to misalignment of cover during installation.

6-17. REMOVAL OF REAR PANEL ASSEMBLY. The rear panel assembly consists of the rear panel, power supply PS1, fan B1, ac filter module A18/J9, fuse F1, the accessory panel, and attaching hardware.

NOTE

The rear panel and the power suppy assembly must be replaced when the power supply is defective.

To remove the rear panel assembly, proceed as follows:

a. Remove top and bottom covers.

b. Remove the screws which attach the accessory panel to the rear panel (MP1, figure 7-6).

c. Remove four machine screws located at the rear of each side panel which attach the side panel to rear corner assemblies (MP1, figure 7-7).

d. Disconnect the connector which carries dc voltages to the Motherboard assembly (PS1J1, figure 6-2).

e. Disconnect the connector which carries ac power to the front panel POWER switch (PS1P1, figure 6-2).

f. Remove the two screws from the brackets that hold PS1 to the main deck (MP3, figure 7-1).

NOTE

The L brackets must remain with the power supply when replacing the rear panel assembly.

g. Slowly remove the rear panel assembly being careful to ease the accessory panel out of the rear panel.

h. Installation is the reverse of the above steps.

6-18. REMOVAL OF FRONT PANEL ASSEMBLY. To remove the front panel assembly, proceed as follows:

a. Remove top and bottom covers.

b. Remove four machine screws located at front of each side panel (MP1, figure 7-7).

c. Remove two screws that hold card cage to the bottom edge of front panel.

d. Disconnect ribbon cable connector P1 from Motherboard CCA (figure 7-13).

e. Disconnect cable W20 from the front panel EXT RF IN connector.

f. Disconnect the connector which carries ac power to the front panel POWER switch (PS1P1, figure 6-2).

g. Disconnect connector P1 from the AC POWER input of the TWTA.

h. Disconnect cable W26 from Step Attenuator AT1 (AT1, figure 7-5).

i. Remove cable W36 from Motherboard CCA connector J12.

j. Installation is the reverse of the above steps.

6-19. REMOVAL OF MECHANICAL RF SWITCHES S9 AND S10. The following is a general procedure to be followed when replacing a defective RF switch.

CAUTION

Be careful not to damage the center conductor when removing or reinstalling SMA cables. Severe VSWR problems may be encountered if these are damaged.

a. Remove top or bottom covers as required.

b. Tag and unsolder all wires connected to the defective switch.

c. Loosen screws holding switch bracket to the chassis to allow for movement. Do not remove screws completely.

d. Progressively loosen and disconnect each cable or RF component connected to the switch being careful not to force anything.

e. When all cables and components have been disconnected, completely remove the bracket screws and remove the switch and bracket.

f. Remove screws holding switch to bracket.

g. Installation is the reverse of the above steps. Tighten all switch cables to 10 $\pm$ 2 inch-pounds.

6-20. REMOVAL OF FIVE-ELEMENT SWITCH/FILTER ASSEMBLY. To remove switch/filter assembly A10, proceed as follows:

a. Remove top and bottom covers.

b. Remove four machine screws on each end of the right side panel (MP1, figure 7-7).

c. Remove four pan head screws from side brace on center of inside panel (MP2, figure 7-7).

d. Lift right side panel off.

e. Disconnect cables W10, W11, and W22 from A10.

f. Tag and unsolder all necessary wires on A10.

g. Remove screws holding A10 to the deck of chassis.

h. Installation is the reverse of the above steps.

6-21. REMOVAL OF THREE ELEMENT SWITCH/FILTER ASSEMBLY. To remove switch/filter assembly A12, proceed as follows:

a. Remove bottom cover.

b. Disconnect RF cables W38 and W12 connected to each end of the bracket assembly (bottom view, figure 7-1).

c. Remove bracket assembly that supports A12 and AR2 by removing two screws (MP1, MP2, figure 7-1).

d. Tag and unsolder the wires connected to A12.

e. Remove four screws holding A12 to bracket.

f. Disconnect A12 from AR2.

CAUTION

Resecure all wires using tie wraps for stress relief.

g. Installation is the reverse of the above steps.

6-22. REMOVAL OF CIRCUIT CARD ASSEMBLIES. The procedure given in this paragraph applies only to those CCAs connected to the Motherboard CCA. The procedure is as follows:

CAUTION

If the Power Meter CCA is defective the entire unit must be returned to depot maintenance.

a. Remove top cover.

b. Remove two machine screws and attaching hardware from top side of card cage assembly and remove side bracket securing CCAs.

c. If the Synthesizer CCA is being replaced, first disconnect cables W1 through W6 that connect to J1 through J6 on the rear side of the board and proceed with step e.

d. If the I/O Extender CCA A6 is being replaced, remove integrated circuit (IC) U4 from its socket in the old board, and insert it into its proper IC socket in the new board (figure 7-16). Verify that jumper wires A, B, and/or C next to U4 are installed in the new board.

NOTE

IC U4 is a memory chip containing programmed instructions for tuning the Power Meter CCA.

e. Hold the defective board from both ends and firmly pull it out of the Motherboard CCA.

f. Installation is the reverse of the above steps.

6-23. REMOVAL OF TWTA. The traveling wave tube amplifier (TWTA) assembly may be removed as follows:

a. Remove top and bottom covers.

b. Disconnect ac power line connected to AC POWER input on top of TWTA.

c. Disconnect RF cables W23 (at RF INPUT) and W24 (at RF OUTPUT) from TWTA.

d. Loosen other end of cables W23 and W24 and move them out of the way.

e. Disconnect cable W9 from amplifier AR4 to allow more room.

f. Remove eight pan head screws at bottom of chassis that hold TWTA in place.

CAUTION

Two of the eight screws also serve to hold a bracket that supports switch/filter A12 and amplifier AR2. Support the bracket during removal of TWTA.

g. Remove TWTA from unit.

h. Installation is the reverse of the above steps.

6-24. REMOVAL OF VCO/SPLITTER ASSEMBLY. The VCO/splitter assembly consists of voltage-controlled oscillator Y1, coupler CP4, and splitter A8 (figure 7-3). To remove any part of this group, proceed as follows:

a. Remove top and bottom covers.

b. Remove four screws from each end of the left side panel.

c. Remove four pan head screws from side brace on center of inside panel (MP1, figure 7-8).

d. Lift left side panel off.

e. Disconnect cable W8 from CP4.

f. Disconnect cable W2 from A8.

g. Disconnect cable W3 from Synthesizer CCA A7.

h. Disconnect cable W7 from Y1.

i. Tag and unsolder wires from Y1.

j. Remove screws from bracket that holds assembly.

k. Disconnect defective part from attached RF components.

l. Installation is the reverse of the above steps.

6-25. REMOVAL OF DOUBLER A11. To remove doubler A11, proceed as follows:

a. Disconnect cable W11 from A11.

b. Disconnect cable W38 from A11.

c. Loosen clamp screws holding A11 to bracket assembly.

d. Installation is the reverse of the above steps.

6-26. REMOVAL OF YIG HARMONIC GENERATOR A13. The YIG harmonic generator consists of a preamplifier (A13A, figure 6-2), a power amplifier (A13B, figure 6-2), and a YIG multiplier (A13C, figure 6-2). All three must be replaced when any one part becomes defective. To remove A13, proceed as follows:

a. Remove top and bottom covers.

b. Disconnect cable W12 from attenuator AT4 (figure 7-1).

c. Disconnect cable W38 from attenuator AT9 (figure 7-1).

d. Disconnect cable W23 from attenuator AT6 and amplifier AR3.

e. Remove six machine screws from top of RF deck that hold A13B and A13C.

f. Disconnect coupler CP7 from A13C.

g. Tag and unsolder wires connected to A13.

h. Installation is the reverse of the above steps.

6-27. REMOVAL OF FREQUENCY DOUBLER A16. To remove frequency doubler A16, proceed as follows:

a. Remove top cover.

b. Disconnect cable W16 from A16J1.

c. Disconnect A16J2 from coupler CP1.

d. Installation is the reverse of the above steps.

6-28. REMOVAL OF FREQUENCY DOUBLER A17. To remove frequency doubler A17, proceed as follows:

a. Remove top cover.

b. Disconnect cable W34 from A17J1.

c. Disconnect A17J2 from switch S10.

d. Installation is the reverse of the above steps.

6-29. REMOVAL OF ASSEMBLIES AR1, AR4, AND A9. Amplifiers AR1 and AR4 and modulator A9 are connected in series next to the TWTA. To remove any part of this group, proceed as follows:

a. Remove top and bottom covers.

b. Disconnect cable W10 from switch/filter A10.

c. Disconnect cable W9 from AR4.

d. Disconnect cable W37 from A9.

e. Remove two screws, at the bottom of deck, that hold AR1.

f. Tag and unsolder wires from defective part.

g. Disconnect defective part from attached RF components.

h. Installation is the reverse of the above steps.

6-30. REMOVAL OF AMPLIFIER AR2. To remove amplifier AR2, proceed as follows:

a. Remove bottom cover.

b. Disconnect attenuator AT9 from amplifier AR2.

c. Disconnect AR2 from switch/filter A12.

d. Tag and unsolder wires from AR2.

e. Installation is the reverse of the above steps.

6-31. REMOVAL OF SWITCH S7. To remove switch S7, proceed as follows:

a. Remove top cover.

b. Disconnect cable W8 from CP4 (figure 7-1).

c. Disconnect cable W9 from S7J1.

d. Disconnect cable W6 from S7J2.

e. Disconnect cable W4 from S7J3.

f. Disconnect cable W5 from S7J4.

g. Remove bracket screw holding S7 to RF deck (MP4, figure 7-1).

h. Tag and unsolder wires and cable W32 from S7.

i. Installation is the reverse of the above steps.

6-32. REMOVAL OF SWITCH S8 AND PIN MODULATOR A14. Mechanical switch S8 and pin modulator A14 are located beneath the three ribbon cables connected to the Motherboard. It is easier to remove both S8 and A14 when either one needs replacement.

a. Remove top and bottom covers.

b. Remove ribbon cables P4, P5, and P6 from the Motherboard.

CAUTION

The pins on P4, P5, and P6 are easily bent. Use special care when removing from or inserting into sockets.

c. Disconnect cable W23 from attenuator AT6.

d. Disconnect cable W14 from switch/filter S10 to allow for movement.

e. Disconnect coupler CP7 from A13C (figure 7-1).

f. Remove bracket screw that holds S8 to RF deck.

g. Disconnect cables W30 and W31 from Motherboard at J9 and J10.

h. Tag and unsolder wires connected to S8.

i. Disconnect defective part from attached RF components.

j. Installation is the reverse of the above steps.

PARTS LIST

CHAPTER 7

PARTS LISTS

7-1. INTRODUCTION. This chapter contains lists of all major parts used in the WJ-1204-1 Synthesized Signal Generator. Included is a list of major units, parts lists, a list of common item descriptions, a list of attaching hardware, a list of manufacturers, and parts location illustrations.

7-2. The information in this chapter is presented primarily in tabular form and provides maintenance parts data to facilitate ready identification of parts for replacement and ordering purposes. It applies to all serial numbers of the WJ-1204-1 Synthesized Signal Generator, which has been manufactured in only one model. The following paragraphs provide instructions for using the various tables in this chapter.

7-3. List of Major Units. Table 7-1 is a list of the major units which comprise the WJ-1204-1 Synthesized Signal Generator according to unit number, nomenclature, and page number. The Unit Number column assigns a numerical designation to each separate unit in the system. Since the WJ-1204-1 consists of only one unit, further references to its constituent parts will omit the "1" designation. For example, instead of refering to the power supply as 1PS1, it will be referred to as PS1.

7-4. The nomenclature column gives the official name of the unit and its type number (model number). The Page Number column lists the number of the first page listing parts for that unit.

7-5. Parts List. Tables 7-2 through 7-6 are the parts lists for the WJ-1204-1. Table 7-2 is the top assembly parts list and is arranged in alphanumeric order. Subsequent tables (7-3 through 7-6) are provided FOR REFERENCE ONLY. Defective circuit card assemblies must be replaced with the exact replacement part.

NOTE

The WJ-1204-1 must be returned to depot maintenance if circuit card assemblies A3 or A6 are faulty.

7-6. Column 1 of each parts list contains the reference designation of all parts listed, in alphanumeric order. Column 2, Notes, references paragraph 7-11 are for explanatory information on a particular part for clarification purposes. Column 3, Name and Description, contains descriptive data to identify the part and aid in determining substitutes. Parts that are used more than five times in the equipment are referenced to table 7-7, List of Common Item Descriptions, for detailed information or, when attaching hardware is involved, to table 7-8, List of Attaching Hardware. For example, capacitor C1 in table 7-3 is referenced to item number 5 in table 7-7, where it is fully described. Column 4, Figure and Item Number, references the parts location illustration by figure number and item number.

7-7. List of Common Item Descriptions. This list, supplied by table 7-7, is provided FOR REFERENCE ONLY and includes the description of multiple use parts (over five applications), except for attaching hardware. All parts are listed in alphabetical order and are assigned an Item Number for reference purposes. Like parts are grouped together and are arranged in order of their

rating. For example, a 10-ohm resistor would be listed first, followed by a 20-ohm, 100-ohm, 1-kilohm, etc.

7-8. List of Attaching Hardware. Standard attaching hardware are listed in table 7-8 when it is used in five or more applications in the equipment. The items are listed FOR REFERENCE ONLY, are arranged in alphabetical order, and are assigned a Letter Code for reference purposes.

7-9. List of Manufacturers. Table 7-9 contains the list of manufacturers that supplied items for manufacturing the equipment. The list includes the name, address, and code number of the manufacturer. The five-digit code is derived from Cataloging Handbook H4-2, Federal Supply Codes for Manufacturers, Code to Name.

7-10. Parts Location Illustrations. Illustrations showing the location of all parts are provided FOR REFERENCE ONLY in figures 7-1 through 7-17.

7-11. Explanation of Notes.

NOTES

1. Table 7-3 provides the parts list for this assembly.
2. Table 7-5 provides the parts list for this assembly.
3. Table 7-6 provides the parts list for this assembly.

Table 7-1. List of Major Units

Unit number	Nomenclature		Page number
	Name of unit	Designation	
1	Synthesized Signal Generator	WJ-1204-1	blank/1-0

Table 7-2. Parts List for WJ-1204-1 Synthesized Signal Generator, Part Number 703051-001, -002

Reference designation	Notes	Name and description	Figure number (item)
1		WJ-1204-1 SYNTHESIZED SIGNAL GENERATOR mfr 14482, part no. 703061-001, -002	6-1, 6-2
A1	1	KEYBOARD CIRCUIT CARD ASSEMBLY mfr 14482, part no. 703085-001.	7-5 (4)
A3		POWER METER CIRCUIT CARD ASSEMBLY; mfr 14482, part no. 703864-002.	7-4
A4		RF CONTROL CIRCUIT CARD ASSEMBLY; mfr 14482, part no. 703077-001.	7-4
A5		DIGITAL CONTROL AND REMOTE INTERFACE CIRCUIT CARD ASSEMBLY; mfr 14482, part no. 703073-001.	7-4
A6	2	I/O EXTENDER CIRCUIT CARD ASSEMBLY; mfr 14482, part no. 703069-001.	7-4
A7	3	SYNTHESIZER CIRCUIT CARD ASSEMBLY; mfr 14482, part no. 703081-001.	7-4
A9		PULSE DRIVER AND MODULATOR; mfr 14482, part no. 703880-001.	7-1 (29)
A10		SWITCH/FILTER; mfr 14482, part no. 703861-001.	7-2 (7)
A12		SWITCH/FILTER; mfr 14482, part no. 703859-001.	7-1 (20)
A13		MULTIPLIER, YIG-TUNED; mfr 14482, part no. 703863-001.	7-1 (24)
A14		PIN LEVELER; mfr 14482, part no. 703881-001.	7-1 (30)
A15		POWER DETECTOR; mfr 14482, part no. 703864-003.	7-1 (18)
A16		DOUBLER/FILTER, 18-26 GHz; mfr 14482, part no. 703867-001.	6-1

Table 7-2. Parts List for WJ-1204-1 Synthesized Signal Generator, Part Number 703051-001, -002 - Continued

Reference designation	Notes	Name and description	Figure number (item)
A17		DOUBLER/FILTER, 13-18 GHz; mfr 14482, part no. 703868-001.	6-1
A20		FRONT PANEL ASSEMBLY; mfr 14482, part no. 703150-001.	7-5, 7-9
AR1		AMPLIFIER, 0.1-1 GHz; mfr 14482, part no. 703877-001.	7-1 (25)
AR2		AMPLIFIER, 0.1-2 GHz; mfr 14482, part no. 703878-001.	7-1 (26)
AR3		TRAVELING WAVE TUBE AMPLIFIER; mfr 14482, part no. 703866-001.	7-1 (23)
AT1		ATTENUATOR (with Cable W27 and panel connector J5); mfr 14482, part no. 703865-001.	7-5 (10)
PS1		POWER SUPPLY; mfr 14482, part no. 703873-002.	7-6 (3)
S7		SWITCH/PIN DIODE LEVELER, SP4T, RF; mfr 14482, part no. 703858-001.	7-1 (19)
S8		SWITCH, RF, SP2T, 2-12 GHz; mfr 14482, part no. 703869-005.	7-1 (21)
S11		SWITCH, RF, SP3T, 0.1-26 GHz, mfr 14482, part no. 703869-001.	7-2 (14)
S12		SWITCH, RF, SP4T, 0.1-26 GHz, mfr 14482, part no. 703869-002.	7-2 (15)
Y1		VCO, 0.5-1 GHz, mfr 14482, part no. 703874-001.	7-3
X3		TRANSFORMER, STEP-DOWN, POWER 230/115 Vac, mfr 14482, part no. 703169	7-7 (12)

Table 7-3. Parts List for Keyboard and Display Circuit Card Assembly A1, Part Number 703085-001

Reference designation	Notes	Name and description	Figure number (item)
A1		KEYBOARD CIRCUIT CARD ASSEMBLY; mfr. 14482, part no. 703085-001	7-12
C1		5	
C2		2	
C3		CAPACITOR, FIXED, CERAMIC DIELECTRIC; 8200 pF, 10%, MIL-C-11015, type CK06BX822K, mfr 81349.	
C4		CAPACITOR, FIXED, CERAMIC DIELECTRIC; 150 pF, 10%, MIL-C-11015, type CK05BX151K, mfr 81349.	
C5		5	
C6		5	
C7		CAPACITOR, FIXED, SOLID ELECTROLYTE, TANTALUM; 4.7 μF, 10%, 10 VDCW, MIL-C-26655, type CS13BC475K, mfr 81349.	
C8		5	
C9		3	
C10		5	
C11		3	
CLR1		MODULE, KEYBOARD; mfr 81073, part no. 82-YY-3601-308.	
CLR2		MODULE, KEYBOARD; mfr 81073, part no. 82-YY-3601-308.	
CLR3		MODULE, KEYBOARD; mfr 81073, part no. 82-YY-3601-308.	
CLR4		11	
CLR5		11	
CLR6		11	

Table 7-3. Parts List for Keyboard and Display Circuit Card Assembly A1, Part Number 703085-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
CLR7		11	
CLR8		11	
CLR9		11	
DS1		8	
DS1MP1		23	
DS2		8	
DS2MP1		23	
DS3		8	
DS3MP1		23	
DS4		8	
DS4MP1		23	
DS5		8	
DS5MP1		23	
DS6		INTEGRATED CIRCUIT, NUMERIC DISPLAY, ±1; mfr 01295, type TIL304.	
DS6MP1		SOCKET, IC, 14-PIN; mfr 01295, part no. C84-14-02.	
DS7		8	
DS7MP1		23	
DS8		8	
DS8MP1		23	
DS9		8	
DS9MP1		23	
DS10		DIODE, LIGHT EMITTING; mfr 50444, part no. 5082-4850.	

Table 7-3. Parts List for Keyboard and Display Circuit Card Assembly A1, Part Number 703085-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
DWN		MODULE, KEYBOARD; mfr 81073, part no. 82-YY-3201-175.	
ENT		MODULE, KEYBOARD; mfr 81073, part no. 82-YY-3201-176.	
J1		CONNECTOR, PRINTED CIRCUIT BOARD, 20-PIN; mfr 75037, part no. 3422-0000T.	
L1		COIL, RADIO FREQUENCY, MOLDED; 0.33 μH, 20%, Military Standard MS18130, part no. MS18130-3, mfr 81349.	
O		MODULE, KEYBOARD; mfr 81073, part no. 82-YY-3601-308.	
P1		EDGE CONNECTOR, 40-PIN; mfr 75037, part no. 3464-0001.	
Q1		TRANSISTOR, JUNCTION FIELD EFFECT, N-CHANNEL; mfr 17856, type 2N4093.	
Q2		TRANSISTOR, NPN; mfr 01295, type 2N2222.	
Q3		TRANSISTOR, NPN; mfr 01295, type 2N2222.	
R1		17	
R2		RESISTOR, FIXED, COMPOSITION; 240 kilohms 5%, 1/4W, MIL-R-39008, part no. RCR07G244JS, mfr 81349.	
R3		RESISTOR, FIXED, COMPOSITION; 220 ohms, 5%, 1/4W, MIL-R-39008, type RCR07G221JS, mfr 81349.	
R4		RESISTOR, FIXED, COMPOSITION, 220 ohms, 5%, 1/4W, MIL-R-39008, type RCR07G221JS, mfr 81349.	
R5		16	
R6		16	
R7		15	

Table 7-3. Parts List for Keyboard and Display Circuit Card Assembly A1, Part Number 703085-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
R8		RESISTOR, VARIABLE; 5 kilohms, 1/2W, MIL-R-22097, type RJ24FP502, mfr 81349.	
R9		RESISTOR, VARIABLE; 1 kilohm, 1/2W, MIL-R-22097, type RJ24FP102, mfr 81349.	
R10		RESISTOR, FIXED, COMPOSITION; 8.2 kilohms, 5%, 1/4W, MIL-R-39008, type RCR07G822JS, mfr 81349.	
R11		RESISTOR, FIXED, COMPOSITION; 1 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G102JS, mfr 81349.	
R12		15	
R13		16	
R14		16	
R15		RESISTOR, FIXED, COMPOSITION; 220 ohms, 5%, 1/4W, MIL-R-39008, type RCR07G221JS, mfr 81349.	
R16		16	
R17		16	
R18		16	
R19		16	
R20		RESISTOR, FIXED, COMPOSITION; 1.1 kilohms, 5%, 1/4W, MIL-R-39008, type RCR07G112JS, mfr 81349.	
R21		17	
R22		16	
R23		16	
R24		16	

Table 7-3. Parts List for Keyboard and Display Circuit Card Assembly A1, Part Number 703085-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
S1		SWITCH; mfr 21251, part no. TE3A.	
TP1		JACK, HORIZONTAL, BLACK; mfr 74970, part no. 105-753-001.	
TP2		JACK, HORIZONTAL, BLACK; mfr 74970, part no. 105-753-001.	
U1		INTEGRATED CIRCUIT, DECODER/ DEMULTIPLEXER; 16-pin, DIP, mfr 01295, type SN74LS138N.	
U2		INTEGRATED CIRCUIT, DUAL 2-LINE-TO-4-LINE DECODER/DEMULTIPLEXER; 16-pin, DIP, mfr 01295, type SN74LS156N.	
U3		INTEGRATED CIRCUIT, TIMER; 8-pin, DIP, mfr 01295, type SN72555N.	
U4		INTEGRATED CIRCUIT, 4-BIT BISTABLE LATCHES; 16-pin, DIP, mfr 01295, type SN74LS375N.	
U5		INTEGRATED CIRCUIT, QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER; 16-pin, DIP, mfr 01295, type SN74LS257N.	
U6		INTEGRATED CIRCUIT, QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER; 16-pin, DIP, mfr 01295, type SN74LS257N.	
U7		INTEGRATED CIRCUIT, QUADRUPLE 2-INPUT POSITIVE-NAND GATES; 14-pin, DIP, mfr 01295, type SN74LS00N.	
U8		INTEGRATED CIRCUIT, CONVERTER, ANALOG-TO-DIGITAL; 18-pin, DIP, mfr 17856, part no. LD130CJ.	
U9		INTEGRATED CIRCUIT, BUS DRIVER, BIDIRECTIONAL, 4-BIT PARALLEL; 16-pin, DIP, mfr 34649, type P8216.	
UP		MODULE, KEYBOARD; mfr 81073, part no. 82-YY-3201-175.	

Table 7-3. Parts List for Keyboard and Display Circuit Card Assembly A1, Part Number 703085-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
VR1		DIODE, ZENER; 6.2V, type 1N825A.	
VR2		DIODE, ZENER; 5.1V, type 1N751A.	

Table 7-4. Parts List for Motherboard Circuit Card Assembly A2, Part Number 703089-001

Reference designation	Notes	Name and description	Figure number (item)
A2		MOTHERBOARD CIRCUIT CARD ASSEMBLY; mfr. 14482, part no. 703089-001	7-13
C1		5	
C2		CAPACITOR, FIXED, CERAMIC DIELECTRIC; 680 pF, 10%, 200V, MIL-C-11015, type CK05BX681K	
C3		3	
C4		CAPACITOR, FIXED, CERAMIC DIELECTIRC; 39 pF, 10%, 200V, MIL-C-11015, type CK06BX103K.	
C5		3	
C6		CAPACITOR, FIXED CERAMIC DIELECTRIC; 22 pF, 10%, 200V, MIL-C-11015, type CK05BX220K	
C7		4	
J1		CONNECTOR, 86 pin; type 1-530677-3, mfr 00779	
J2		CONNECTOR, 86 pin; type 1-530677-3, mfr 00779	
J3		CONNECTOR, 86 pin; type 1-530677-3, mfr 00779	
J4		CONNECTOR, 86 pin; type 1-530677-3, mfr 00779	
J5		CONNECTOR, 36 pin; type 1-530677-5, mfr 00779	
J6		TEST SOCKET, 24 pin; type C8324-02, mfr 01295	
J7		CONNECTOR, SMA, PWB, RIGHT ANGLE; type 50-653-0000, mfr 98291	
J8		CONNECTOR, SMC, PWB, RIGHT ANGLE; type 50-053-0000, mfr 98291	
J9		CONNECTOR, SMC, PWB, RIGHT ANGLE; type 50-053-0000, mfr 98291	

Table 7-4. Parts List for Motherboard Circuit Card Assembly A2, Part Number 703089-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
J10		CONNECTOR, SMC, PWB, RIGHT ANGLE; type 50-053-0000, mfr 98291	
J11		CONNECTOR, SMA, PWB, RIGHT ANGLE; type 50-653-0000, mfr 98291.	
J12		CONNECTOR, SMA, PWB, RIGHT ANGLE; type 50-6-3-0000, mfr 98291.	
L1		COIL; 560 μH, 10%, type MS90537-46.	
L2		COIL; 560 μH, 10%, type MS90537-46.	
R1		RESISTOR, FIXED COMPOSITION; 220 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G224JS.	
R2		RESISTOR, FIXED COMPOSITION; 11 kilohm, 5%, MIL-R-39008, type RCR07G113JS.	
R3		RESISTOR, FIXED COMPOSITION; 11 kilohm, 5%, MIL-R-39008, type RCR07G113JS	
R4		18	
R5		RESISTOR, FIXED COMPOSITION; 220 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G224JS.	
R6		12	
R7		12	
R8		17	
R9		RESISTOR, FIXED COMPOSITION; 1.5 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G152JS.	
R10		RESISTOR, FIXED COMPOSITION; 2 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G202JS.	
R11		RESISTOR, FIXED COMPOSITION; 27 ohm, 5%, 1/4W, MIL-R-39008, type RCR07G322JS.	
R12		RESISTOR, FIXED COMPOSITION; 3.2 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G322JS	

Table 7-4. Parts List for Motherboard Circuit Card Assembly A2, Part Number 703089-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
RP1		RESISTOR, SIP; 3.3 ohm, type 784-1-R3.3K.	
RP2		RESISTOR, SIP; 200 ohm, type 784-1-R220.	
RP3		RESISTOR, SIP; 220 ohm, type 784-1-R220.	
U1		IC; type LH0004CH, mfr 27014.	
U2		DIODE ARRAY; type TID-130, mfr 01295.	
VR1		ZENER DIODE, 15V; type IN5245.	
VR2		VOLTAGE REGULATOR; type 78M20UC, mfr 07263.	
XA1		KEY, CONNECTOR; type 530687-1, mfr 00779.	
XA2		KEY, CONNECTOR; type 530687-1, mfr 00779	
XS1		SOCKET, DIP.	

Table 7-5. Parts List for I/O Extender Circuit Card Assembly A6, Part Number 703069-001

Reference designation	Notes	Name and description	Figure number (item)
A6		I/O EXTENDER CIRCUIT CARD ASSEMBLY; mfr. 14482, part no. 703069-001	7-16
C1		CAPACITOR, FIXED, SOLID ELECTROLYTE, TANTALUM; 10 μF, 10%, 20W, Vdc, MIL-C-26655, type CS13BE106K	
C2		CAPACITOR, FIXED, SOLID ELECTROLYTE, TANTALUM; 4.7 μF, 10%, 10W, Vdc, MIL-C-26655, type CS13BC475K.	
C3		CAPACITOR, FIXED, SOLID ELECTROLYTE, TANTALUM; 10 μF, 10%, 20W, Vdc, MIL-C-26655, type CS13BE106K.	
C4		3	
C5		5	
C6		5	
C7		3	
C8		5	
C9		5	
C10		1	
C11		4	
C12		5	
C13		5	
C14		5	
C15		5	
C16		4	
C17		4	
C18		5	

Table 7-5. Parts List for I/O Extender Circuit Card Assembly A6, Part Number 703069-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
C19		5	
C20		4	
C21		4	
C22		4	
C23		4	
C24		4	
C25		4	
C26		4	
C27		4	
C28		4	
L1		CHOKE, 3.3 μH, 10%, type MS18130-14	
L2		CHOKE, 0.33 μH, 20%, type MS18130-5.	
L3		CHOKE, 3.3 μH, 10%, type MS18130-14	
L4		CHOKE, 3.3 μH, 10%, type MS18130-14.	
R19		22	
R20		RESISTOR, FIXED COMPOSITION; 75 kilohm, 5%, 1.4W, MIL-R-39008, type RCR0753JS.	
R21		RESISTOR, VARIABLE; 50 kilohm, 1/2W, MIL-R-22097, type RJ24FX503.	
R22		RESISTOR, FIXED COMPOSITION; 24 kilohm, 5%, 1.4W, MIL-R-39008, type RCR0753JS.	
R23		18	
R24		RESISTOR, FIXED COMPOSITION; 330 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G334JS.	

Table 7-5. Parts List for I/O Extender Circuit Card Assembly A6, Part Number 703069-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
R25		RESISTOR, FIXED COMPOSITION; 2.7 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G272JS.	
R26		22	
R27		22	
R28		22	
R29		22	
R30		22	
R31		22	
R32		22	
R33		22	
R34		RESISTOR, FIXED COMPOSITION; 110 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G114JS.	
R35		16	
R36		14	
R37		14	
R38		RESISTOR, VARIABLE; 5 kilohm, type 1240X5K, mfr 18612.	
R39		RESISTOR, FIXED COMPOSITION; 110 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G114JS.	
RP1		RESISTOR PAK; 4.7 kilohm, type 898-1-R4.7K, mfr 06110.	
RP2		RESISTOR PAK; 100 ohm, type 316B101, mfr 01121.	
RP3		RESISTOR PAK; 100 ohm, type 314B101, mfr 01121.	
TP1		JACK, HORIZONTAL, BLACK; type 105-753-001, mfr 74970.	

Table 7-5. Parts List for I/O Extender Circuit Card Assembly A6, Part Number 703069-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
TP2		JACK, HORIZONTAL, WHITE; type 105-751-001, mfr 74970.	
TP3		JACK, HORIZONTAL, BROWN; type 105-758-001, mfr 74970.	
TP4		JACK, HORIZONTAL, RED; type 105-752-001, mfr 74970.	
TP5		JACK, HORIZONTAL, GREEN; type 105-754-001, mfr 74970.	
TP6		JACK, HORIZONTAL, YELLOW; type 105-757-001, mfr 74970.	
U1		IC, 8 CHANNEL, MOS ANALOG MULTIPLEXER; type AM3705C, mfr 27014.	
U2		IC, 8 CHANNEL, MOS ANALOG MULTIPLEXER; type AM3705C, mfr 27014.	
U3		IC, DIGITAL ANALOG CONVERTER; type DAC-022CCX1, mfr 06665.	
U4		IC, PROGRAMMABLE READ ONLY MEMORY; type 6349-1, mfr 63491.	
U5		9	
U6		9	
U7		9	
U8		9	
U9		IC, DIGITAL/ANALOG CONVERTER; type DAC-70C-BCD-1, mfr 13919.	
U10		IC, DIGITAL ANALOG CONVERTER; type DAC-022CCX1, mfr 06665.	
U11		IC, OPERATIONAL AMPLIFIER; type OP-07CJ, mfr 06665.	
U12		10	

Table 7-5. Parts List for I/O Extender Circuit Card Assembly A6, Part Number 703069-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
U13		10	
U14		10	
U15		10	
J16		IC, TRANSISTOR ARRAY; type ULN2001A, mfr 13606.	
U17		10	
U18		10	
U19		10	
U20		10	
U21		IC, TRANSISTOR ARRAY; type 2001A, mfr 13606.	
VR2		ZENER DIODE; 4.7V, type IN750A	
VR3		ZENER DIODE; 5.1V, type IN751A	
XU4		SOCKET, LOW PROFILE; 20 pin, type C83-20-02, mfr 01295.	
XU9		SOCKET, LOW PROFILE; 24 pin, type C83-24-02, mfr 01295.	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001

Reference designation	Notes	Name and description	Figure number (item)
A7		SYNTHESIZER CIRCUIT CARD ASSEMBLY; mfr. 14482, part no. 703081-001	7-17
AR1		IC, OPERATIONAL AMPLIFIER; type LM101AH, mfr 27014.	
AR2		IC, OPERATIONAL AMPLIFIER, type LM101AH, mfr 27014.	
AR3		IC, COMPARATOR, type LM319H, mfr 27014.	
AR4		IC, OPERATIONAL AMPLIFIER, type LM101AH, mfr 27014.	
AR1MP1		INSULATING PAD, TO-99; type RCT05140-8A.	
AR2MP1		INSULATING PAD,TO-99; type RCT05140-8A.	
AR3MP1		INSULATING PAD, TO-100, type RCT05140-10A.	
AR4MP1		INSULATING PAD, TO-99; type RCT05140-8A.	
C1		CAPACITOR, FIXED, SOLID ELECTROLYTE, TANTALUM, 1.0 μF, 50W, Vdc, MIL-C-26655, type CS13BG105K.	
C2		CAPACITOR, FIXED, SOLID ELECTROLYTE, TANTALUM, 33 μF, 10W, Vdc, MIL-C-26655, type CS13BG336K.	
C3		4	
C6		11	
C7		1	
C8		1	
C9		1	
C10		1	
C11		1	
C12		1	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
C13		1	
C14		1	
C15		1	
C16		1	
C17		1	
C18		1	
C19		1	
C20		1	
C21		1	
C22		2	
C23		1	
C24		1	
C25		1	
C26		1	
C27		4	
C28		1	
C29		2	
C30		5	
C31		4	
C32		2	
C33		4	
C34		4	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
C35		CAPACITOR, FIXED, CERAMIC, DIELECTRIC (GENERAL PURPOSE); 390 pF, 200W, Vdc, MIL-C-11015, type CK05BX1K.	
C36		4	
C37		CAPACITOR, FIXED, CERAMIC, DIELECTRIC (GENERAL PURPOSE); 390 pF, 200W, Vdc, MIL-C-11015, type CK05BX1K.	
C38		2	
C39		CAPACITOR, FIXED CERAMIC, DIELECTRIC (GENERAL PURPOSE); 4700 pF, 200W, Vdc, MIL-C-11015, type CK06BX472K.	
C40		CAPACITOR, FIXED CERAMIC, DIELECTRIC (GENERAL PURPOSE); 0.47 μF, 50W, Vdc, MIL-C-11015, type CK06BX474K.	
C41		4	
C42		4	
C43		4	
C45		4	
C46		4	
C47		4	
C48		4	
C49		4	
C50		CAPACITOR, FIXED SOLID ELECTROLYTE, TANTALUM; 1.0 μF, 50W, Vdc, MIL-C-26655, type CS13BG105K	
C51		4	
C52		2	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
C53		CAPACITOR, FIXED SOLID ELECTROLYTE, TANTALUM; 1.0 μF, 50W, Vdc, MIL-C-26655, type CS13BG105K.	
C54		4	
C55		2	
C56		CAPACITOR, FIXED SOLID ELECTROLYTE, TANTALUM; 33 μF, 10W, Vdc, MIL-C-26655, type CS13BG336K.	
C57		4	
C58		2	
C59		3	
C60		3	
C61		CAPACITOR, FIXED CERAMIC, DIELECTRIC (GENERAL PURPOSE); 0.47 μF, 50W, Vdc, MIL-C-11015, type CK06BX474K.	
C62		CAPACITOR, FIXED CERAMIC, DIELECTRIC (GENERAL PURPOSE); 390 pF, 220W, Vdc, MIL-C-11015, type CK05BX1K.	
C63		4	
C64		CAPACITOR, FIXED CERAMIC, DIELECTRIC (GENERAL PURPOSE); 4700 pF, 200W, Vdc, MIL-C-11015, type CK06BX472K.	
C65		4	
C66		5	
C67		4	
C68		5	
C69		4	
C70		4	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
C71		4	
C72		4	
C73		2	
C74		2	
C75		2	
C76		2	
C77		2	
C78		2	
C79		2	
CR1		ZENER DIODE; 6.8V, type IN957B.	
CR2		DIODE; type IN914.	
CR3		DIODE; type IN914.	
CR4		DIODE; type IN914.	
CR5		DIODE; type IN914.	
CR6		DIODE; type IN914.	
CR7		DIODE; type IN914.	
J1		CONNECTOR, RF, PC MOUNT; type 50-651-0000-31, mfr 98921.	
J2		CONNECTOR, RF PC MOUNT; type 50-651-0000-31, mfr 98921.	
J3		CONNECTOR, RF, PC MOUNT; type 50-651-0000-31, mfr 98921.	
J4		CONNECTOR, RF, PC MOUNT; type 50-651-0000-31, mfr 98921.	
J5		CONNECTOR, RF, PC MOUNT; type 50-651-0000-31, mfr 98921.	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
J6		CONNECTOR, RF, PC MOUNT; type 50-651-0000-31, mfr 98921.	
L1		INDUCTOR; 0.22 μH, 10%, type S18130-2.	
L2		INDUCTOR; 33 μH, 10%, type MS18130-26.	
L3		INDUCTOR; 0.22 μH, 10%, type S18130-2.	
L4		INDUCTOR; 33 μH, 10%, type MS18130-26.	
L5		INDUCTOR; 33 μH, 10%, type MS18130-26.	
(Q1)		INSULATING PAD, TO-5; type 10027-DAP, mfr 07047.	
(Q2)		INSULATING PAD, TO-5; type 10027-DAP, mfr 07047.	
R1		RESISTOR, FIXED COMPOSITION; 100 ohm, 5%, 1/4W, MIL-R-39008, type RCR32G101JS.	
R2		13	
R3		RESISTOR, FIXED COMPOSITION; 36 ohm, 5%, 1/4W, MIL-R-39008, type RCR07G360JS.	
R4		13	
R5		15	
R6		15	
R7		RESISTOR, FIXED COMPOSITION; 51 ohm, 5%, 1/4W, MIL-R-39008, type RCR07510JS.	
R8		13	
R9		13	
R10		18	
R11		18	
R12		18	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
R13		18	
R14		12	
R15		19	
R16		RESISTOR, FIXED COMPOSITION; 5.1 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G512JS.	
R17		RESISTOR, FIXED COMPOSITION, VARIABLE; 20 kilohm, MIL-R-22097, type RJ24FX203K.	
R18		RESISTOR, FIXED COMPOSITION; 5.1 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G512JS.	
R19		15	
R20		19	
R21		19	
R22		15	
R23		RESISTOR, FIXED COMPOSITION; 2 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G512JS.	
R24		RESISTOR, FIXED COMPOSITION; 5.1 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G512JS.	
R25		RESISTOR, FIXED COMPOSITION; 2 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G512JS.	
R26		RESISTOR, FIXED COMPOSITION; 2 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G512JS.	
R27		14	
R28		RESISTOR, FIXED COMPOSITION; 5.1 kilohms, 5%, 1/4W, MIL-R-39008, type RCR07G512JS.	
R29		RESISTOR, FIXED COMPOSITION; 30 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G303JS.	
R30		RESISTOR, VARIABLE; 50 kilohm, MIL-R-22097, type RJ24FX503K.	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
R31		18	
R32		14	
R33		14	
R34		RESISTOR, FIXED COMPOSITION; 4.3 kilohm, 5%, 1/4W, type RCR07G432JS.	
R35		RESISTOR, FIXED COMPOSITION; 6.8 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G682JS.	
R36		RESISTOR, FIXED COMPOSITION; 9.1 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G912JS.	
R37		RESISTOR, FIXED COMPOSITION; 15 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G153JS.	
R38		14	
R39		12	
R40		12	
R41		12	
R42		12	
R43		12	
R44		12	
R45		19	
R46		RESISTOR, FIXED COMPOSITION; 470 ohm, 1/4W, 5%, MIL-R-39008, type RCR07G471JS.	
R47		RESISTOR, FIXED COMPOSITION; 430 ohm, 5%, 1/4W, MIL-R-39008, type RCR07G431JS.	
R48		13	
R49		13	
R50		17	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001-Continued

Reference designation	Notes	Name and description	Figur numbe (item
R51		14	
R52		14	
R53		17	
R54		RESISTOR, FIXED COMPOSITION; 36 ohm, 5%, 1/4W, MIL-R-39008, type RCR07G360JS.	
R55		13	
R56		13	
R57		14	
R58		14	
R59		15	
R60		15	
R61		15	
R62		15	
R63		19	
R64		19	
R65		19	
R66		RESISTOR, FIXED COMPOSITION; 30 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G303JS.	
R67		19	
R68		12	
R69		18	
R70		18	
R71		RESISTOR, FIXED COMPOSITION, 30 kilohm, 5%, 1/4W, MIL-R-39008, type RCR07G303JS.	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
R72		12	
RP2		21	
RP3		21	
RP4		21	
RP5		21	
RP6		21	
RP7		21	
RP8		21	
RP9		21	
RP10		21	
RP11		21	
RP12		21	
RP13		21	
RP14		21	
RP15		21	
RP16		21	
TP0		HORIZONTAL JACK, BLACK; type 105-753-001, mfr 74970.	
TP1		HORIZONTAL JACK, BROWN; type 105-758-001, mfr 74970.	
TP2		HORIZONTAL JACK, RED; type 105-752-001, mfr 74970.	
TP3		HORIZONTAL JACK, ORANGE; type 105-756-001, mfr 74970.	
TP4		HORIZONTAL JACK, YELLOW; type 105-757-001, mfr 74970.	

Table 7-6. Parts List for Synthesizer Circuit Card Assembly A7, Part Number 703081-001-Continued

Reference designation	Notes	Name and description	Figure number (item)
U1		IC, 1 GHz, DIVIDER; type SP8609B, mfr 52648.	
U2		IC, 500 MHz DIVIDER; type SP8602, mfr 52648.	
U3		IC, 300 MHz DIVIDER; type SP8604, mfr 52648.	
U4		IC, ECL OR/NOR; type F95105DC, mfr 07263.	
U5		7	
U6		7	
U7		7	
U8		7	
U9		7	
U10		IC, ECL DIVIDE BY 10 OR 11; type 11C90DC.	
U11		IC, ECL OR/NOR; type F95109DC.	
U12		IC, ECL OR/NOR; type F95105C, mfr 07263.	
U13		IC, ECL, DIVIDE BY 10 OR 11; type 11C90DC.	
U14		IC, ECL OR/NOR; type F95105C, mfr 07263.	
U15		7	
U16		7	
U17		7	
U18		IC, ECL PHASE DETECTOR; type MC12040L, mfr 04713.	
U19		6	
U20		IC, 5 MHz REFERENCE OSCILLATOR; type CO231-T-4, mfr 27802.	
U21		6	
U22		6	
U23		IC, 1 GHz DIVIDER; type SP8609B, mfr 52648.	

Table 7-7. List of Common Item Descriptions

Item number	Description
1	CAPACITOR, FIXED, CERAMIC DIELECTRIC; 100 pF, 200 VDCW, MIL-C-11015, type CK05BX101K, mfr. 81349.
2	CAPACITOR, FIXED, CERAMIC DIELECTRIC; 1000 pF, 200 VDCW, MIL-C-11015, type CK05BX102K, mfr. 81349.
3	CAPACITOR, FIXED, CERAMIC DIELECTRIC; 0.01 μF, 200 VDCW, MIL-C-11015, type CK06BX103K, mfr. 81349.
4	CAPACITOR, FIXED, CERAMIC DIELECTRIC; 0.1 μF, 100 VDCW, MIL-C-11015, type CK06BX104K, mfr. 81349.
5	CAPACITOR, FIXED, CERAMIC DIELECTRIC; 1 μF, 50 VDCW, MIL-C-11015, type CK06BX105K, mfr. 81349.
6	INTEGRATED CIRCUIT, ANALOG SWITCH; mfr. 24355, type DG201BJ.
7	INTEGRATED CIRCUIT, DECADE DIVIDER, ECL; mfr. 07263, type F95010.
8	INTEGRATED CIRCUIT, NUMERIC DISPLAY WITH LOGIC; mfr. 01295, type TIL308.
9	INTEGRATED CIRCUIT, PROGRAMMABLE PERIPHERAL INTERFACE; mfr. 34649, type 8255A.
10	INTEGRATED CIRCUIT, TRANSLATOR, HIGH SPEED DUAL LEVEL; mfr. 27014, type DH0034CD.
11	MODULE, KEYBOARD; mfr. 81073, part no. 82-YY-3601-68.
12	RESISTOR, FIXED, COMPOSITION; 100 ohms, 5%, 1/4W, MIL-R-39008, type RCR07G101JS, mfr. 81349.
13	RESISTOR, FIXED, COMPOSITION; 150 ohms, 5%, 1/4W, MIL-R-39008, type RCR07G151JS, mfr. 81349.
14	RESISTOR, FIXED, COMPOSITION; 200 ohms, 5%, 1/4W, MIL-R-39008, type RCR07G201JS, mfr. 81349.
15	RESISTOR, FIXED, COMPOSITION; 510 ohms, 5%, 1/4W, MIL-R-39008, type RCR07G511JS, mfr. 81349.
16	RESISTOR, FIXED, COMPOSITION; 4.7 kilohms, 5%, 1/4W, MIL-R-39008, type RCR07G472JS, mfr. 81349.

Table 7-7. List of Common Item Descriptions - Continued

Item number	Description
17	RESISTOR, FIXED, COMPOSITION; 10 kilohms, 5%, 1/4W, MIL-R-3900 type RCR07G103JS, mfr. 81349.
18	RESISTOR, FIXED, COMPOSITION; 20 kilohms, 5%, 1/4W, MIL-R-39008, type RCR07G203JS, mfr. 81349.
19	RESISTOR, FIXED, COMPOSITION; 100 kilohms, 5%, 1/4 W, MIL-R-39 type RCR07G104JS, mfr. 81349.
20	RESISTOR, FIXED, HIGH STABILITY; 34 kilohms, 1%, 1/8W, MIL-R-10509, type RN60C3402F, mfr. 81349.
21	RESISTOR PAK; 470 ohm, mfr. 32997, part no. 4306R-101-471.
22	RESISTOR, VARIABLE; 10 kilohms, 1/2W, MIL-R-22097, type RJ24FX103, mfr. 81349.
23	SOCKET, IC, 16-PIN; mfr. 01295, part no. C84-16-02.

Table 7-8. List of Attaching Hardware

Letter code	Name and description
A	NUT, SELF-LOCKING, 8-32; part no. MS21044-CO3
B	NUT, SELF-LOCKING, #4; part no. MS21044-CO4
C	NUT, SELF-LOCKING, #6; part no. MS21044-CO6
D	NUT, 6-32; part no. MS35649-264
E	SCREW, PAN HD, 2-56 X 5/16; part no. MS51957-4
F	SCREW, PAN HD, 4-40 X .5 LG; part no. MS51957-17
G	SCREW, PAN HD, 4-40 X .75 LG; part no. MS51957-19
H	SCREW, PAN HD, 4-40 X .38 LG; part no. MS51957-15
I	SCREW, PAN HD, 4-40 X 1.25 LG; part no. MS51957-22
J	SCREW, PAN HD, 4-40 X 1; part no. MS51957-21
K	SCREW, PAN HD, 6-32 X .50 LG; part no. MS51957-30
L	SCREW, PAN HD, 6-32 X 1.25; part no. MS51957-35
M	SCREW, PAN HD, 8-32 X 1.25; part no. MS51957-50
N	WASHER, FLAT, #4; part no. AN960-C4L
O	WASHER, FLAT #6; part no. AN960-C6L
P	WASHER, FLAT #8; part no. AN960-C8
Q	WASHER, LOCK #2; part no. MS35338-134

Table 7-9. List of Manufacturers

Code	Manufacturer
00779	AMP Inc. P. O. Box 3608 Harrisburg, PA 17105
01121	Allen-Bradley Co. 1201 2nd St. South Milwaukee, WI
01295	Texas Instruments Inc. Semiconductor Group P. O. Box 5012 13500 N. Central Expressway Dallas, TX 75222
04713	Motorola Inc. Semiconductor Products Div. 5005 E. McDowell Road Phoenix, AZ 85036
06110	Fairchild Controls Div of Fairchild Camera and Instrument Corp. Mountain View, CA
07047	The Milton Ross Co. 511 Second Street Pike Southampton, PA 18966
07126	Digitran Co., The 855 South Arroyo Parkway Pasadena, CA 91105
07263	Fairchild Camera and Instrument Corp. Semiconductor Division 464 Ellis St. Mountain View, CA 94042
10133	XLO Micromatic 45 E. 48th St. Holland, MI 49423
12136	PHC Industries Inc. 1643 Haddon Ave. Camden, NJ 08103
13103	Thermally Co. Inc. P. O. Box 34829 2021 W. Valley View Lane Dallas, TX

Table 7-9. List of Manufacturers -Continued

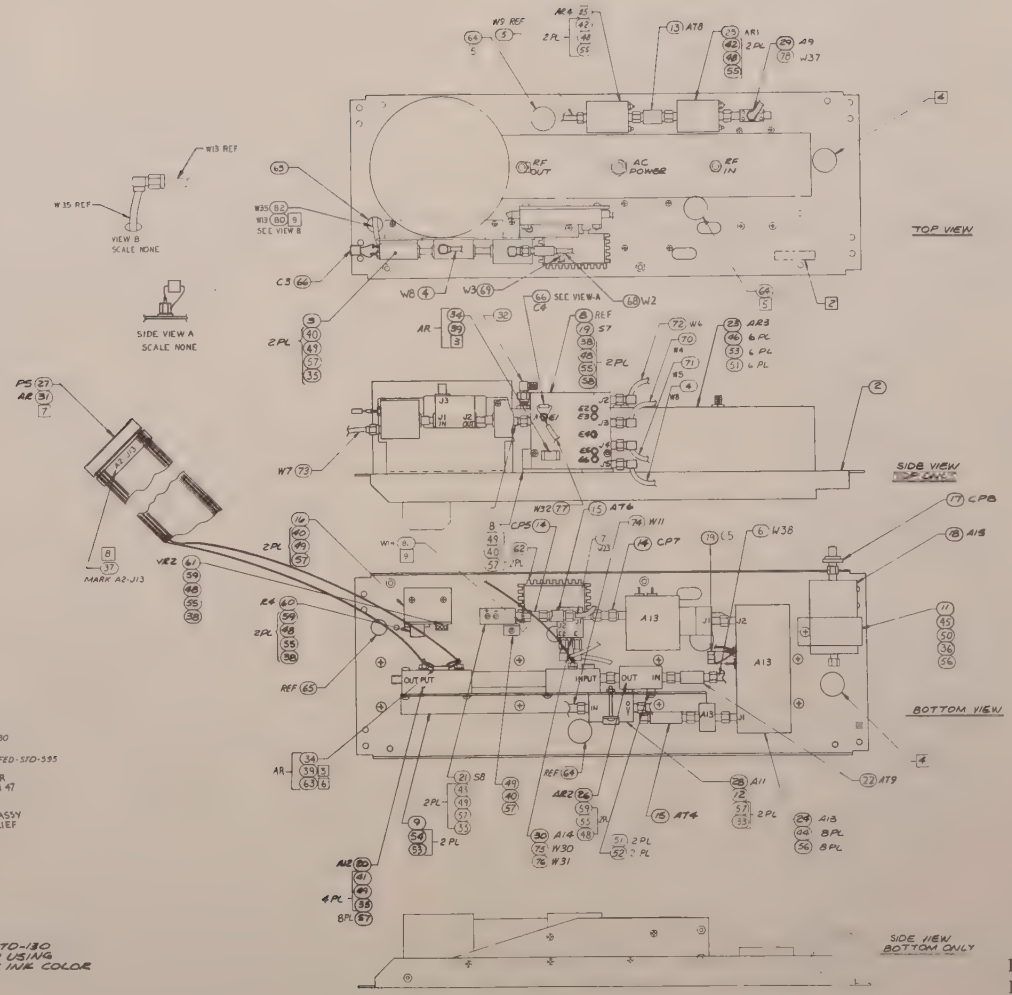
Code	Manufacturer
13606	Sprague Electric Co. Transistor Division Pemcroke Rd Concord, NH 03301
13919	Burr-Brown Research Corp P. O. Box 11400 6730 S. Tucson Blvd. Tucson, AZ 85706
14482	Watkins-Johnson Co. 3333 Hillview Ave. Palo Alto, CA 94304
17856	Siliconix Inc. 2201 Laurelwood Rd. Santa Clara, CA 95054
18612	Vishay Resistor Products Div. Vishay Intertechnology Inc. 63 Lincoln Hwy Malvern, PA 19355
18915	Birtcher Corp, The Industrial Div. 4371 Valley Blvd Los Angeles, CA 90032
19080	Robinson Electronics Inc. 3580 Sacramento Drive San Luis Obispo, CA 93401
21251	Arrow Electronics Inc. 3100 Plainfield Rd. Dayton, OH 45432
21604	Buckeye Stamping Co. 555 Marion Road Columbus, OH 43207
23936	Pamotor Div. William J. Purdy Co. 770 Airport Blvd. Burlingame, CA 94010
24355	Analog Devices Inc. P. O. Box 280 Rt. 1 Industrial Park Norwood, MA 02062

Table 7-9. List of Manufacturers -Continued

Code	Manufacturer
27014	National Semiconductor Corp. 2900 San Ysidro Way Santa Clara, CA 95051
27802	Vectron Laboratories Inc. 121 Water St. Norwalk, CT 06854
28480	Hewlett-Packard Co., Corporate Hq. 1501 Page Mill Rd. Palo Alto, CA 94304
32559	Bivar Inc. 1617 E. Edinger Ave. Santa Ana, CA 92705
32767	Griffith Plastics Corp. P. O. Box 4365 1027 California Drive Burlingame, CA 94010
32997	Bourns Inc., Trimpot Products Div. 1200 Columbia Ave. Riverside, CA 92507
34649	Intel Corp. 3065 Bowers Ave. Santa Clara, CA 95051
50364	Monolithic Memories Inc. 1165 E. Arques Ave. Sunnyvale, CA 94086
50444	Hewlett-Packard Co., H-P Laboratories 1501 Page Mill Rd. Palo Alto, CA 94304
52648	Plessey Memories Inc. DBA Plessey Semiconductors 1674 McGraw Ave. Santa Ana, CA 92705
74970	E.F. Johnson Co. 299 10th Ave. S.W. Waseca, MN 56093

Table 7-9. List of Manufacturers -Continued

Code	Manufacturer
75037	Minnesota Mining and Mfg Co. Electro Products Div. 3M Center St. Paul, MN
77122	Palnut Co., The A United-Carr Div. of TRW Inc. Glen Rd. Mountainside, NJ
78553	Eaton Corp Engineered Fasteners Div. Tinnerman Plant P.O. Box 6688 8700 Brookpark Rd. Cleveland, OH 44101
81073	Grayhill Inc. P.O. Box 373 561 Hillgrove Ave. La Grange, IL 60525
81349	Military Specifications Promulgated by Military Departments/ Agencies under Authority of Defense Standardization Manual 4120 3-M
83330	Herman H. Smith Inc. 812 Snediker Ave. Brooklyn, NY 11207
93459	Weinschel Engineering Co., Inc. P.O. Box 577 Clopper Road Gaithersburg, MD 20760
95077	Solitron/Microwave Div. Solitron Devices Inc. P.O. Box 278 Cove Road Port Salerno, FL 33492
98921	O and M Mfg. Co. 8203 Market St. Road P.O. Box 24098 Houston, TX 77029



9 CONNECT ONLY 1 END AT THIS ASSY LEVEL. THE FREE END WILL NOT BE CONNECTED UNTIL THE TOP ASSY 703051-001

8 MARK INDICATED REF DESIGNATION PER MIL-STD-130 APPROXIMATELY WHERE SHOWN USING .12 HIGH CHARACTERS WITH WHITE INK COLOR NO 17873 PER FED-STD-595

7 WIRE ACCORDING TO WIRE LIST 703148 SOLDER PER MIL-ST-454 REQUIREMENT 5, USING ITEM 47 DO NOT SHRINK SLEEVING AT THIS LEVEL

6 SECURE INDIVIDUAL WIRES FROM RIBBON CABLE ASSY TO ITEM 34 USING ITEM 63, FOR STAIN RELIEF

5 TRIM TO FIT IF NECESSARY

4 CLEARANCE HOLES ARE SHOWN FOR ORIENTATION OF RF COMPONENTS

3 BOND ITEM 34 TO ITEM 8 USING ITEM 39 CLEAN ALL SURFACES WITH ALCOHOL PRIOR TO BONDING.

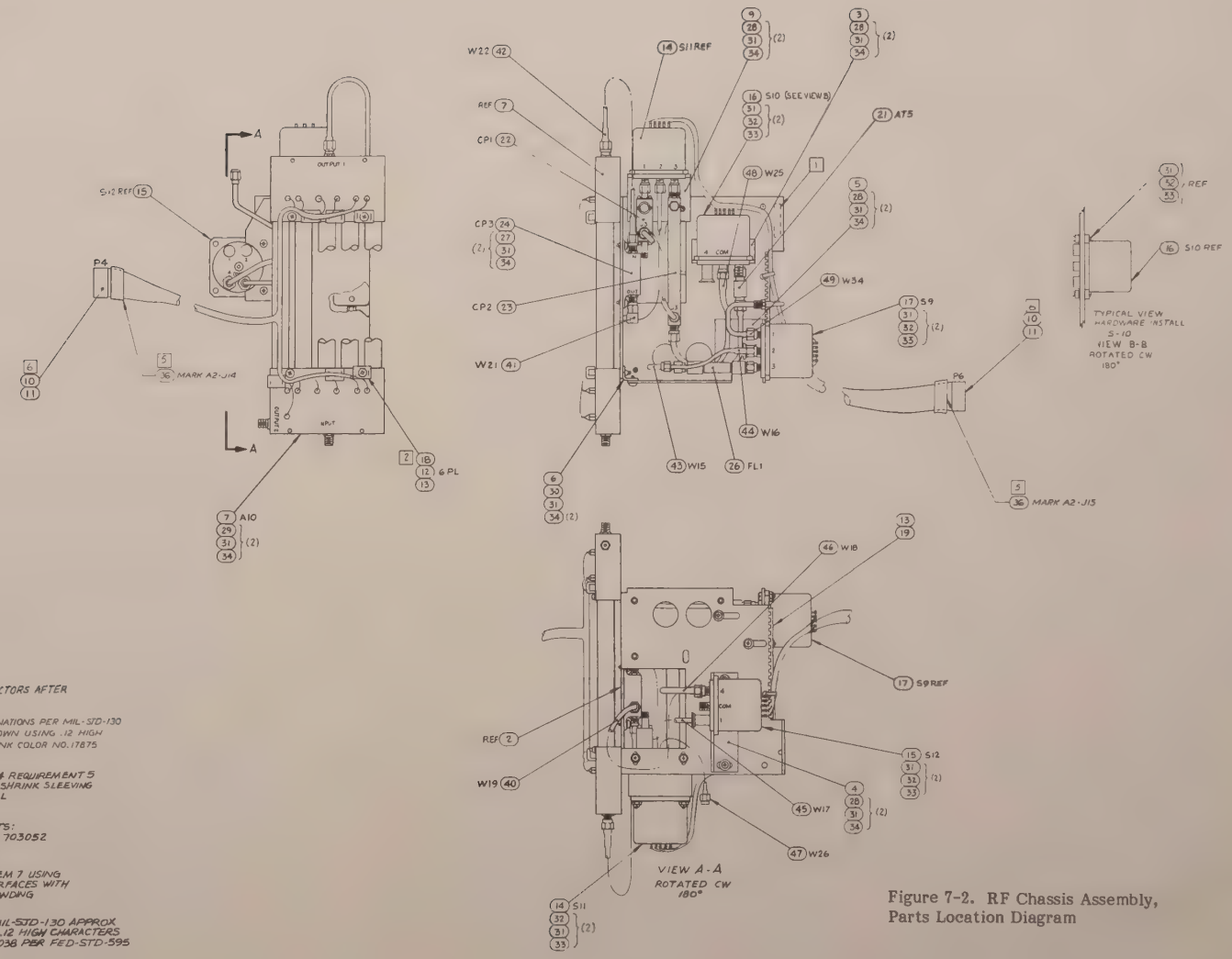
2 MARK ASSY NUMBER PER MIL-STD-130 APPROXIMATELY WHERE SHOWN USING .12 HIGH CHARACTERS WITH BLK INK COLOR 37038 PER FED-STD-595

1 REFERENCE DOCUMENTS:
SCHEMATIC DIAGRAM 703052
WIRE LIST 703148

NOTES UNLESS OTHERWISE SPECIFIED

703148E

Figure 7-1. RF Deck Assembly, Parts Location Diagram



6. INSTALL P4 AND P6 CONNECTORS AFTER LEVEL II ASSY

5. MARK INDICATED REF DESIGNATIONS PER MIL-STD-130 APPROXIMATELY WHERE SHOWN USING .12 HIGH CHARACTERS WITH WHITE INK COLOR NO.17875 PER FED-STD-595

4. SOLDER PER MIL-STD-454 REQUIREMENT 5 USING ITEM 50. DO NOT SHRINK SLEEVING AT THIS ASSEMBLY LEVEL

3. REFERENCE DOCUMENTS: SCHEMATIC DIAGRAM 703052 WIRE LIST 703148

2. BOND ITEM 12 TO ITEM 7 USING ITEM 13. CLEAN ALL SURFACES WITH ALCOHOL PRIOR TO BONDING

1. MARK PART NO. PER MIL-STD-130 APPROX WHERE SHOWN USING .12 HIGH CHARACTERS WITH BLK INK COLOR 17038 PER FED-STD-595

NOTES: UNLESS OTHERWISE SPECIFIED

703141C

Figure 7-2. RF Chassis Assembly, Parts Location Diagram

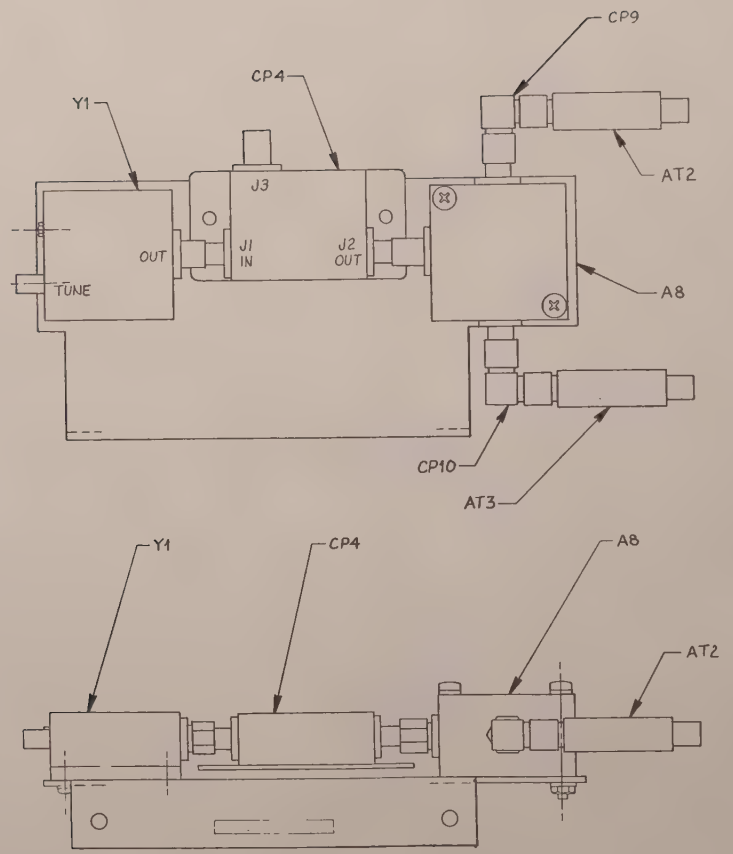
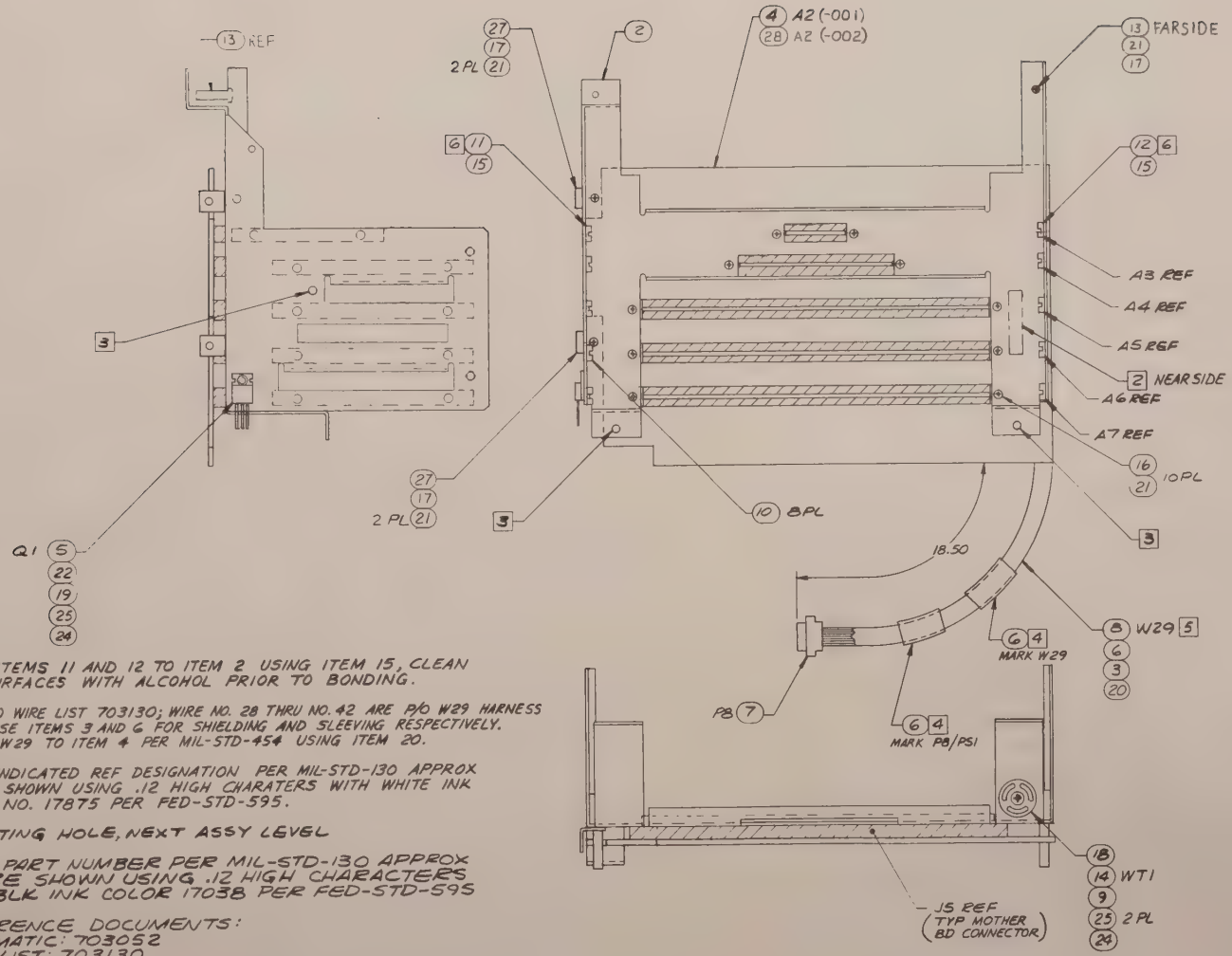


Figure 7-3. VCO/Splitter Assembly, Parts Location Diagram

79-L-072
(703139A)



6 BOND ITEMS 11 AND 12 TO ITEM 2 USING ITEM 15, CLEAN ALL SURFACES WITH ALCOHOL PRIOR TO BONDING.

5 REFER TO WIRE LIST 703130; WIRE NO. 28 THRU NO. 42 ARE P/O W29 HARNESS ASSY. USE ITEMS 3 AND 6 FOR SHIELDING AND SLEEVING RESPECTIVELY. SOLDER W29 TO ITEM 4 PER MIL-STD-454 USING ITEM 20.

4 MARK INDICATED REF DESIGNATION PER MIL-STD-130 APPROX WHERE SHOWN USING .12 HIGH CHARATERS WITH WHITE INK COLOR NO. 17875 PER FED-STD-595.

3 MOUNTING HOLE, NEXT ASSY LEVEL

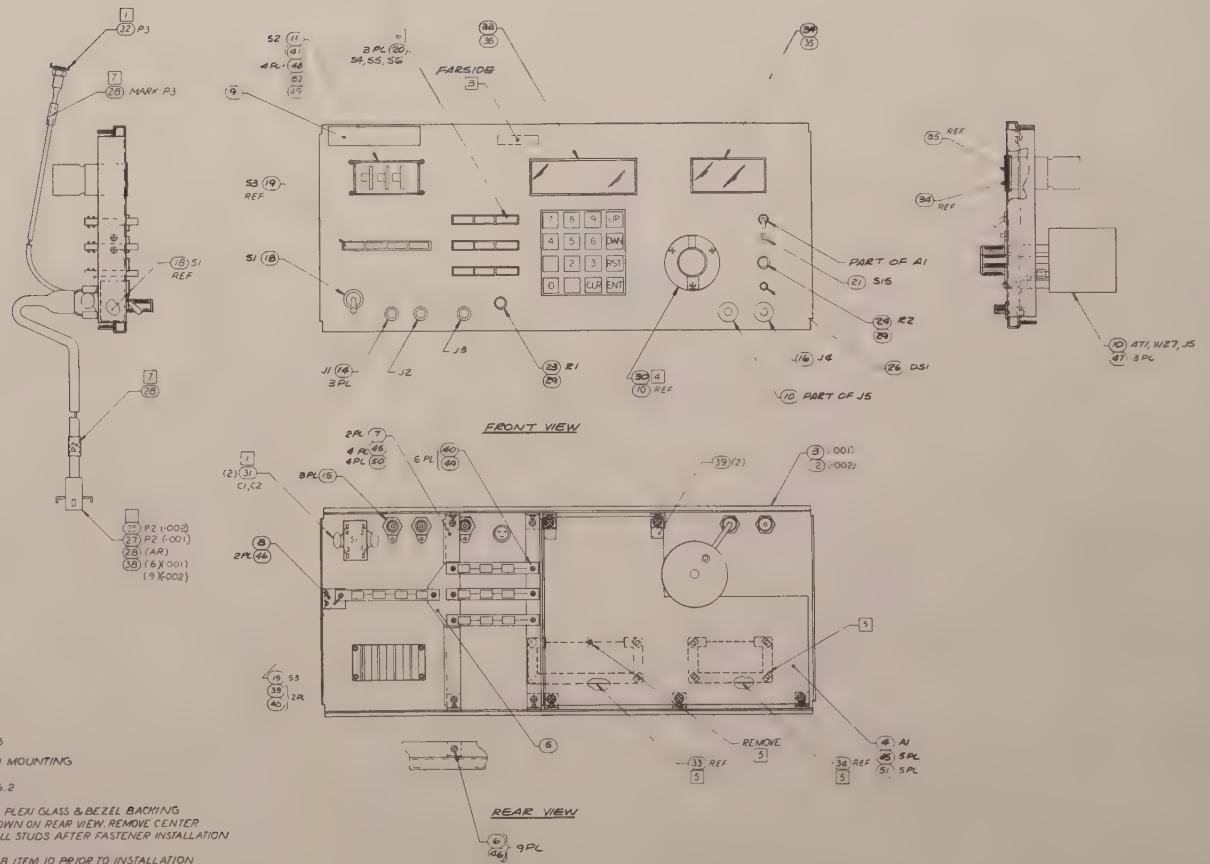
2 MARK PART NUMBER PER MIL-STD-130 APPROX WHERE SHOWN USING .12 HIGH CHARACTERS WITH BLK INK COLOR 17038 PER FED-STD-595

1 REFERENCE DOCUMENTS:
SCHEMATIC: 703052
WIRE LIST: 703130

NOTES: UNLESS OTHERWISE SPECIFIED

703147E

Figure 7-4. Card Cage Subassembly, Parts Location Diagram



[7] MARK INDICATED REF DES PER MIL-STD-130 APPROX WHERE SHOWN USING .12 HIGH CHARACTERS WITH WHITE INK COLOR NO.17875 PER FED-STD-595

[6] TRIM SHADE CONTACTS EVEN WITH MOUNTING BAR, ITEMS 19 AND 20. SEE WIRING LIST WL 703150 FIG. 2

[5] INSTALL GASKET IN BETWEEN RED PLEXI GLASS & BEZEL BACKING PLATE. CUT BACKING PLATE AS SHOWN ON REAR VIEW. REMOVE CENTER STUD AT THE BOTTOM AND TRIM ALL STUDS AFTER FASTENER INSTALLATION

[4] REMOVE EXISTING INDICATOR KNOB, ITEM 10, PRIOR TO INSTALLATION

[3] MARK ASSY NO. PER MIL-STD-130 APPROX WHERE SHOWN USING .12 HIGH CHARACTERS WITH BLK INK COLOR 17038 PER FED-STD-595

2 SOLDER PER MIL-STD-454 REQUIREMENT 5 USING ITEM 37

[1] REFERENCE DOCUMENTS: INTERCONNECT DIAGRAM 703052 WIRE LIST 703150 MACHINE FEATURE INDEX 703171

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 7-5. Front Panel Assembly, Parts Location Diagram

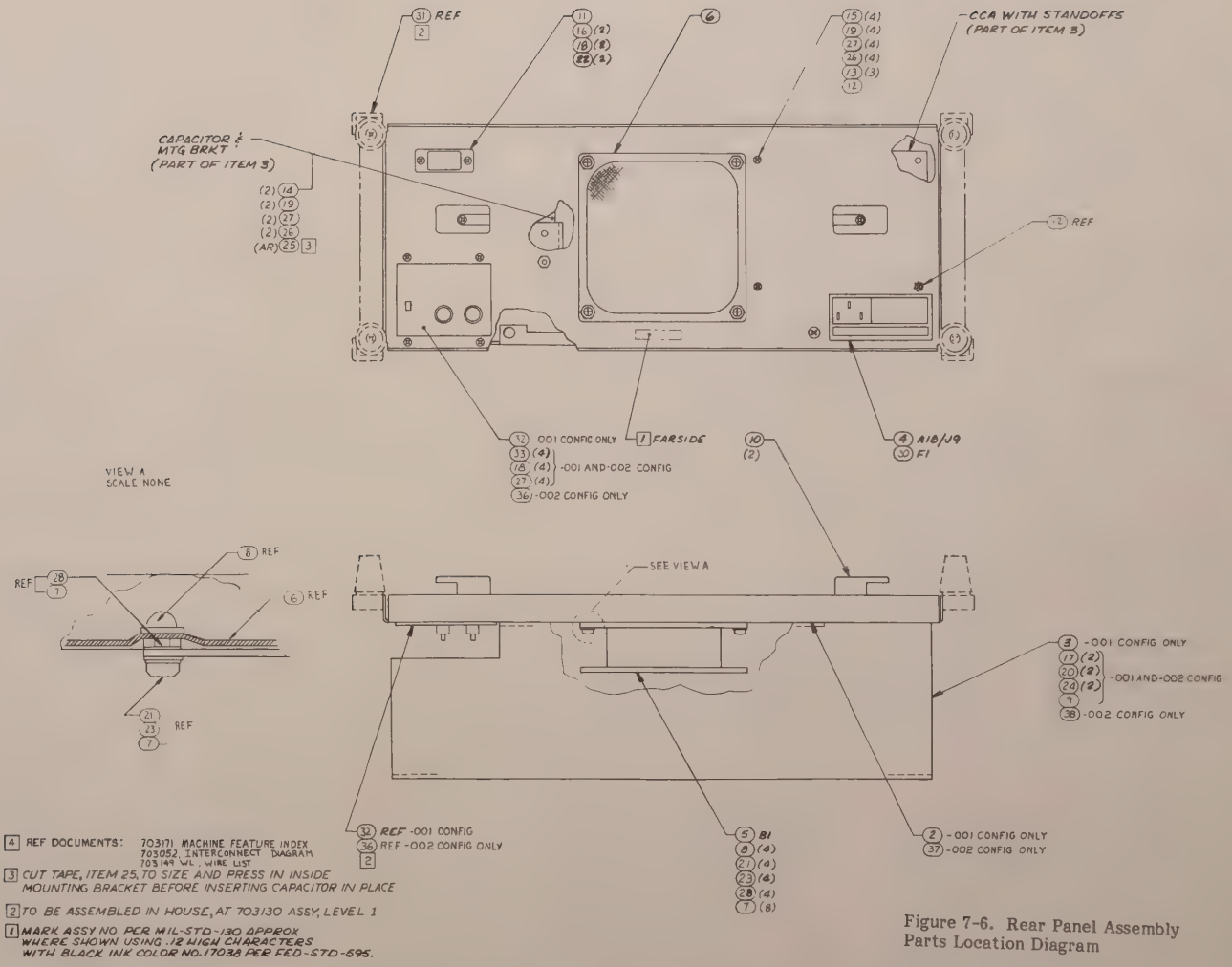


Figure 7-6. Rear Panel Assembly Parts Location Diagram

703149D

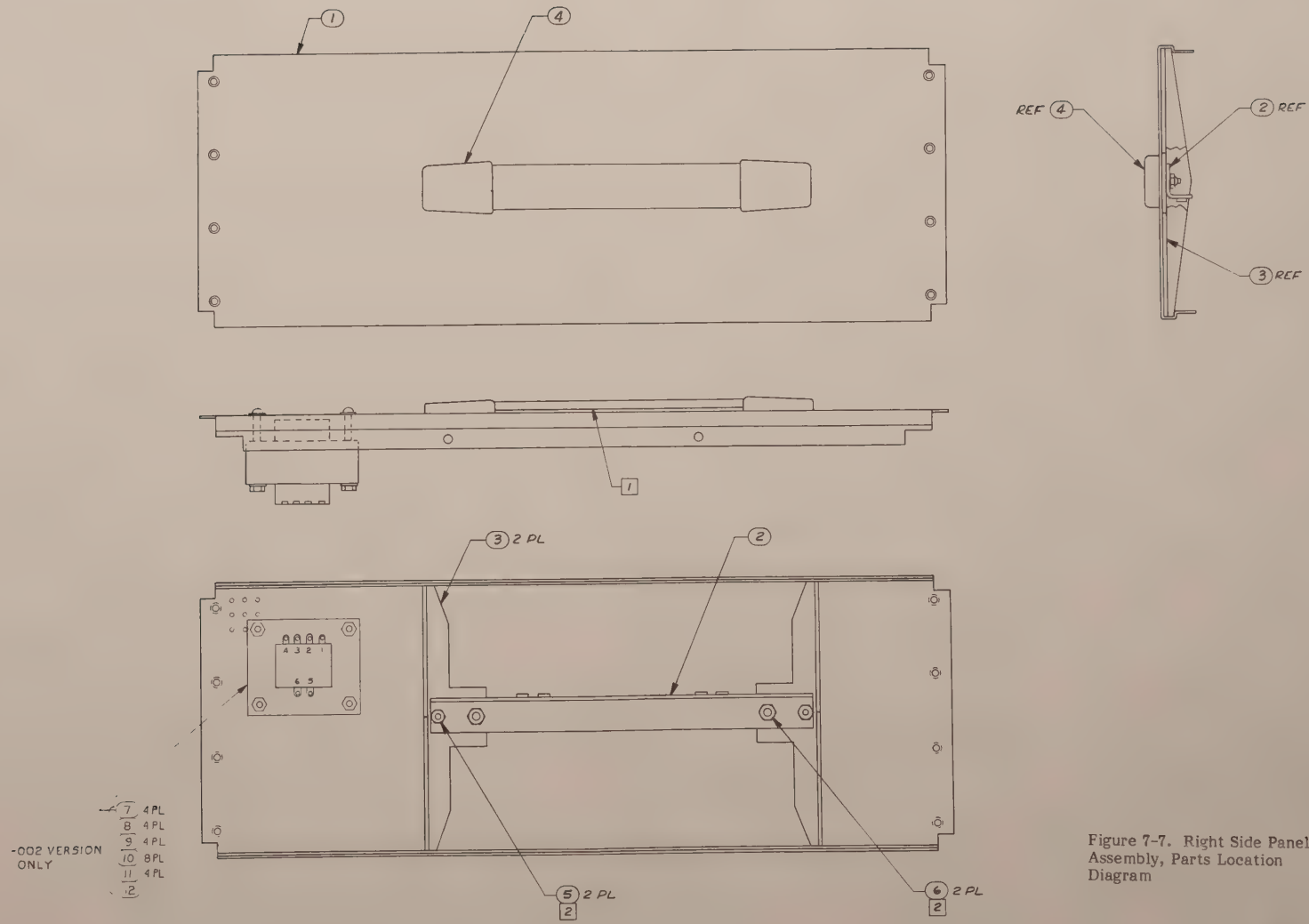


Figure 7-7. Right Side Panel Assembly, Parts Location Diagram

703100B

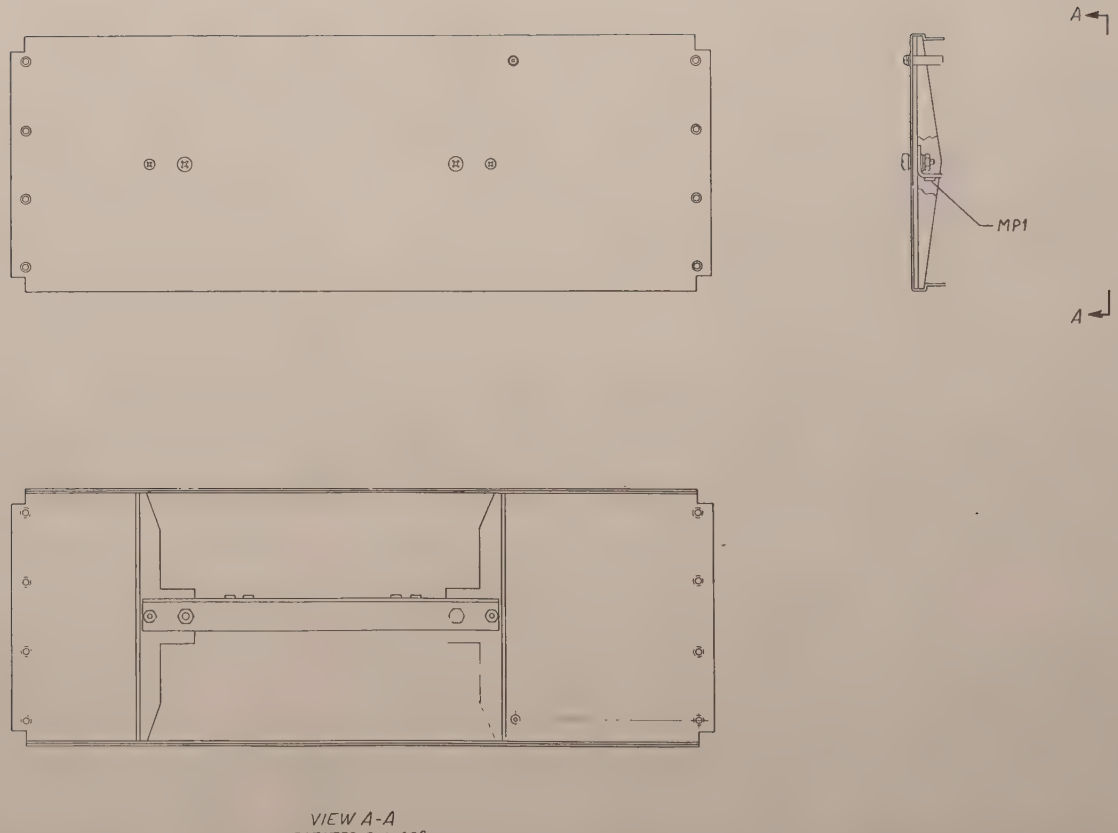


Figure 7-8. Left Side Panel Assembly, Parts Location Diagram

79-L-077
(703146A)

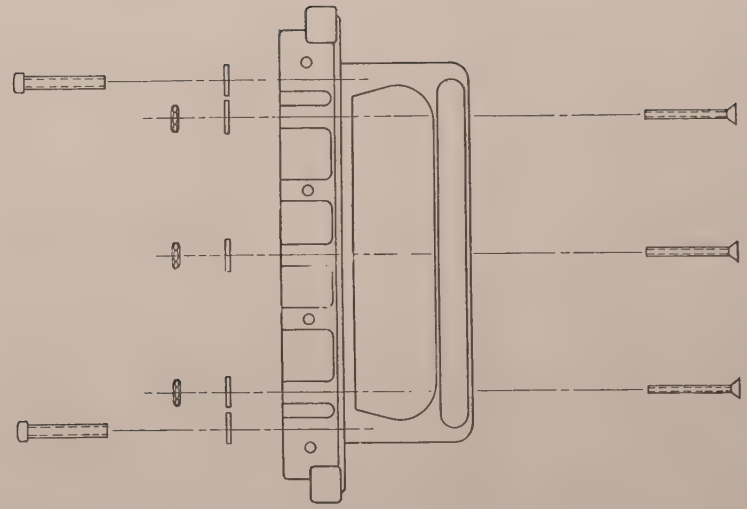


Figure 7-9. Front Corner Panel Assembly, Parts Location Diagram

79-L-078
(703145A)

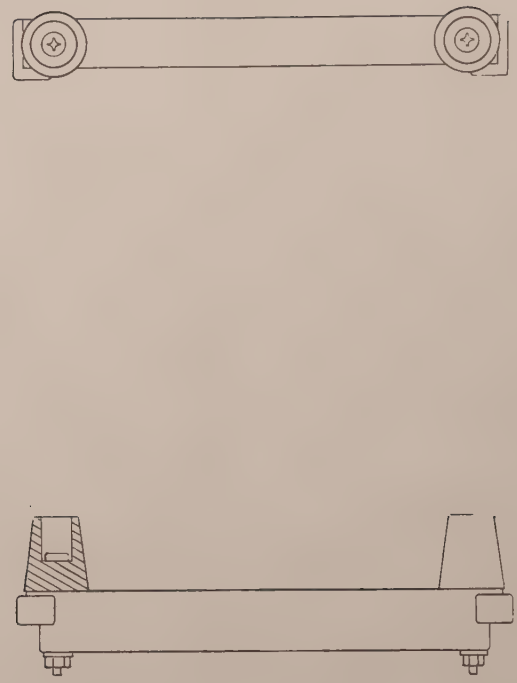
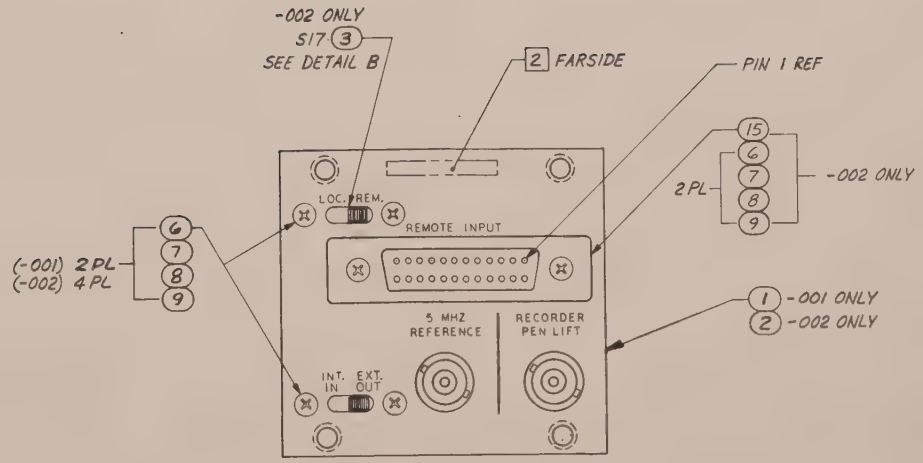
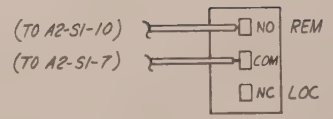


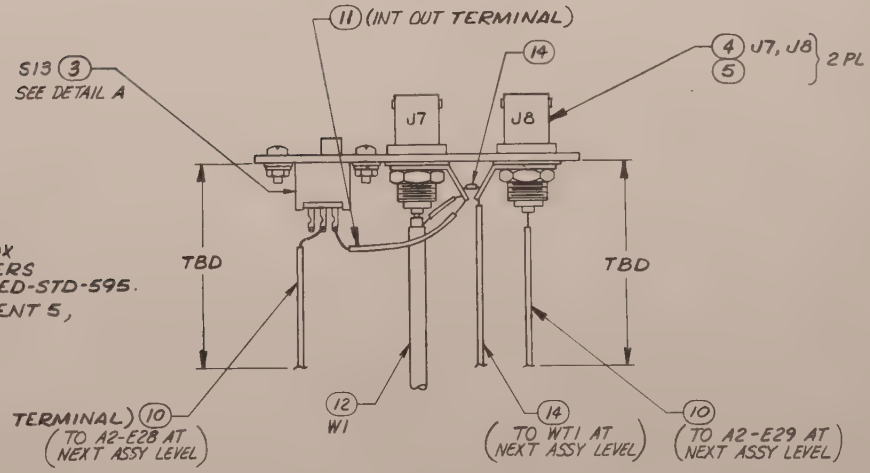
Figure 7-10. Rear Corner Panel Assembly, Parts Location Diagram

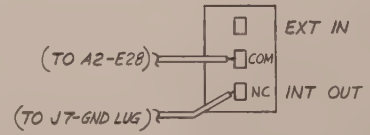
79-L-079
(703144A)





DETAIL B : S17 REAR VIEW
SCALE: NONE
-002 ONLY





DETAIL A : S13 REAR VIEW
SCALE: NONE

[2] MARK ASSY NO. PER MIL-STD-130 APPROX WHERE SHOWN USING .12 HIGH CHARACTERS WITH BLACK INK COLOR NO. 17038 PER FED-STD-595.

1. SOLDER PER MIL-STD-454, REQUIREMENT 5, USING ITEM 13.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 7-11. Accessory Panel Assembly, Parts Location Diagram

703127

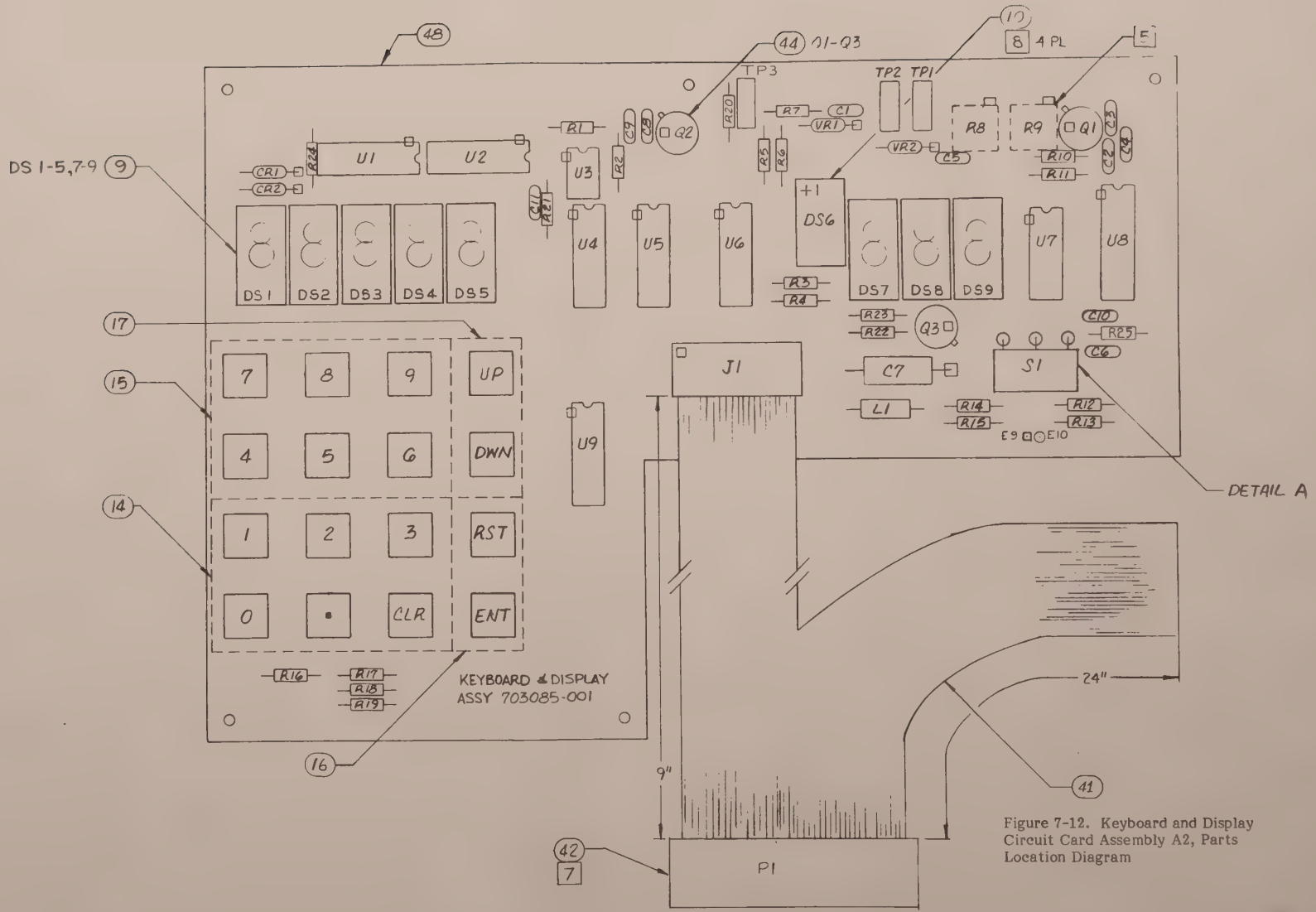


Figure 7-12. Keyboard and Display Circuit Card Assembly A2, Parts Location Diagram

703085D

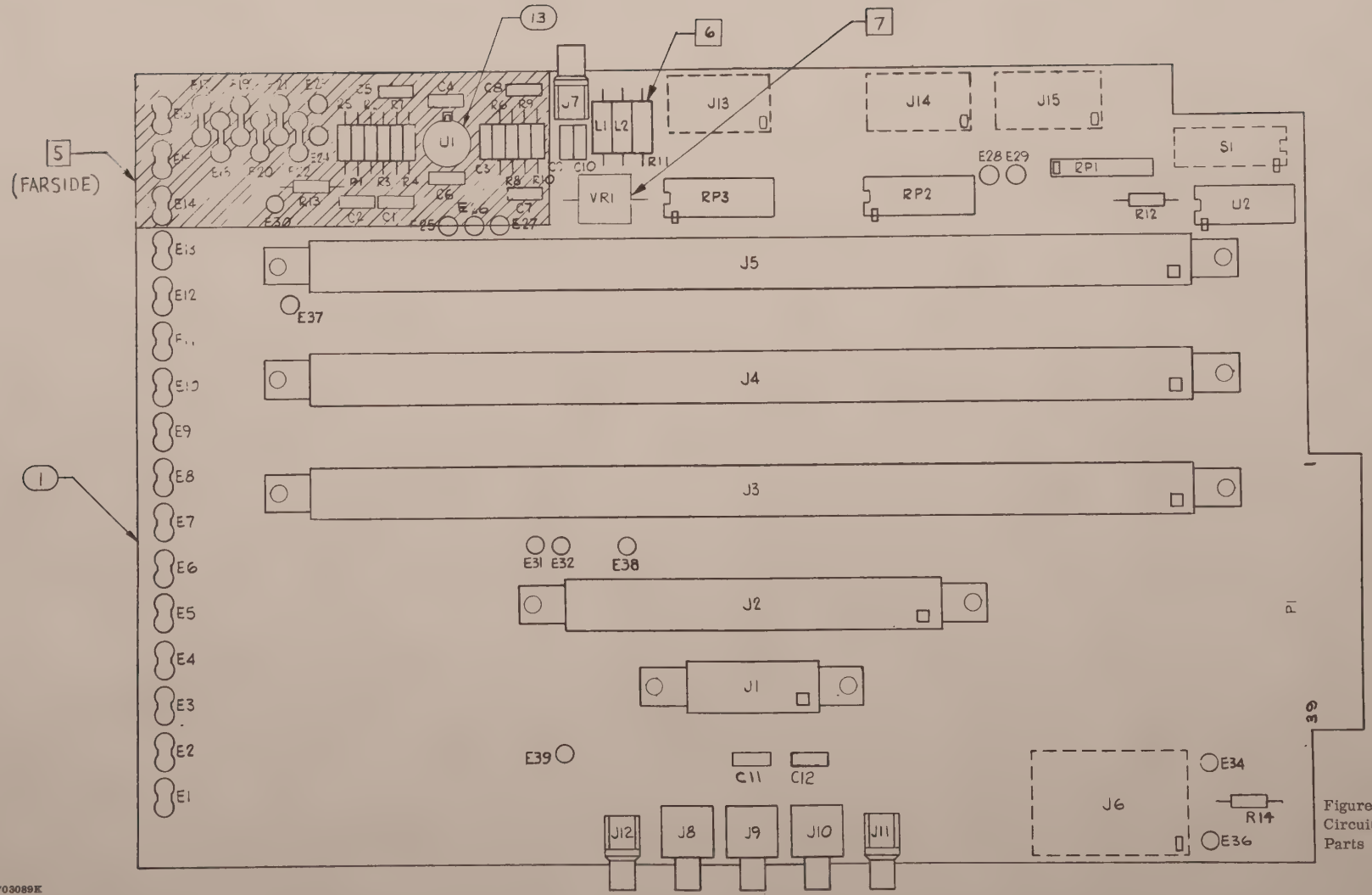


Figure 7-13. Motherboard Circuit Card Assembly A2, Parts Location Diagram

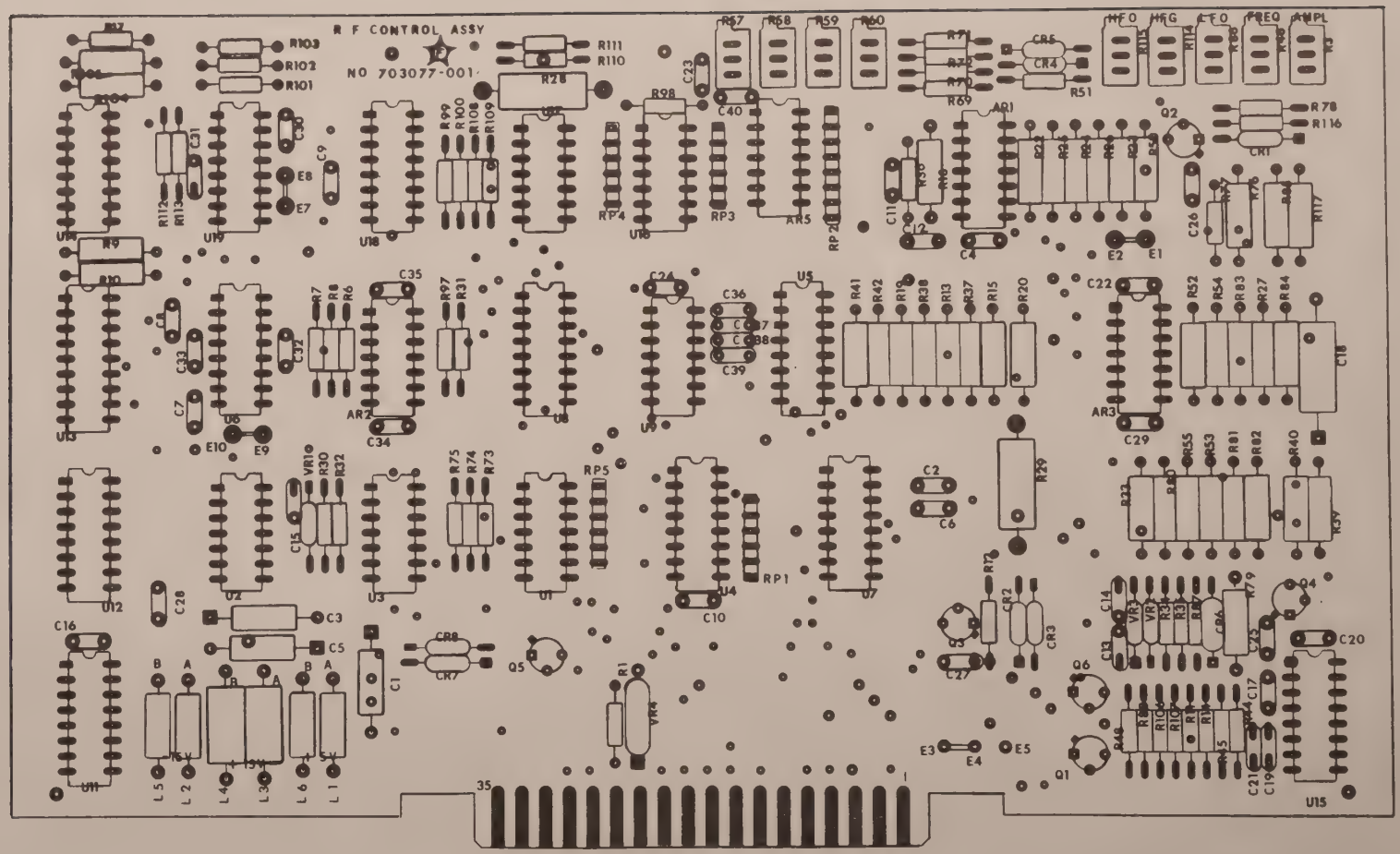


Figure 7-14. RF Control Circuit Card Assembly A4, Parts Location Diagram

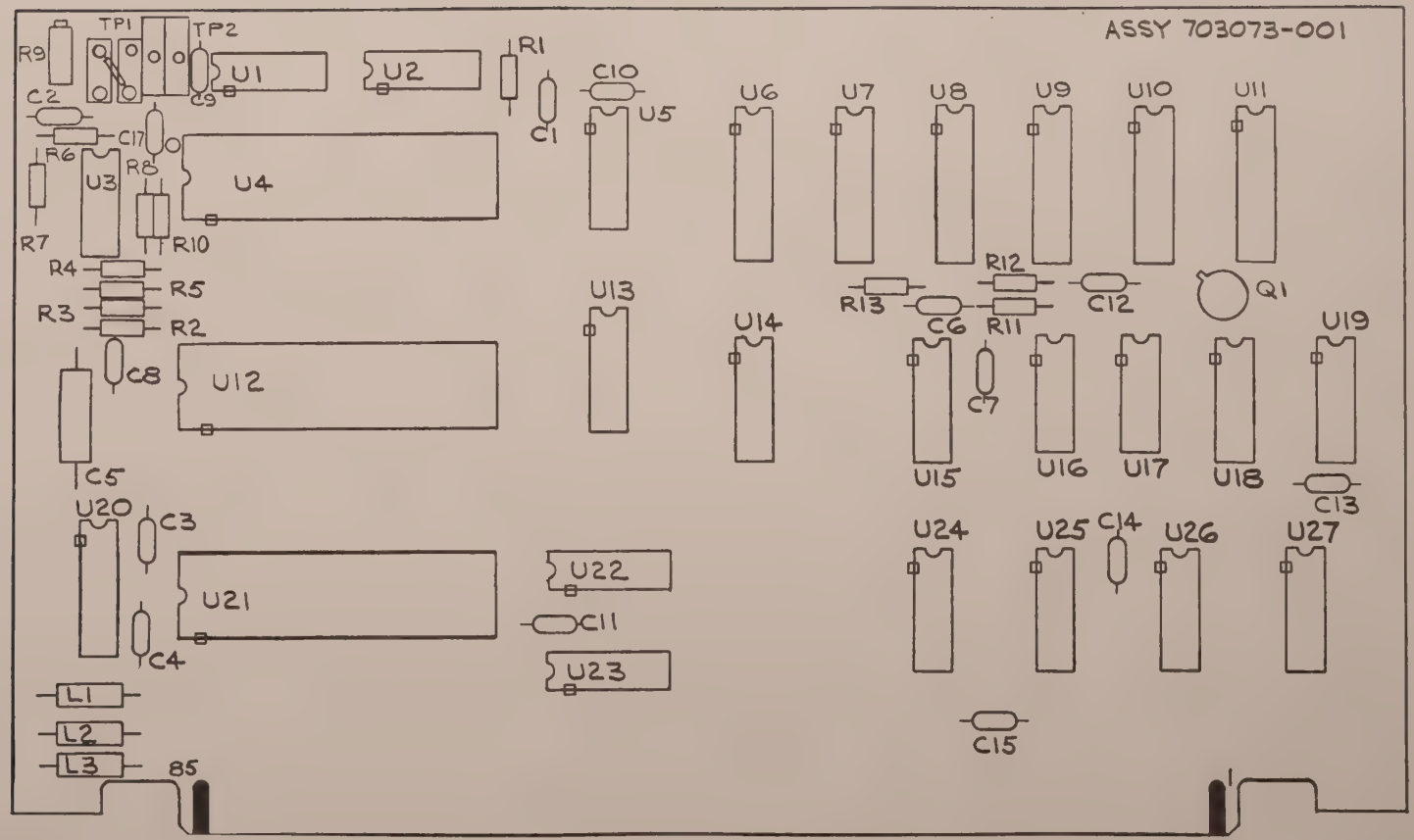


Figure 7-15. Digital Control and Remote Interface Circuit Card Assembly A5, Parts Location Diagram

79-L-002
(703073A)

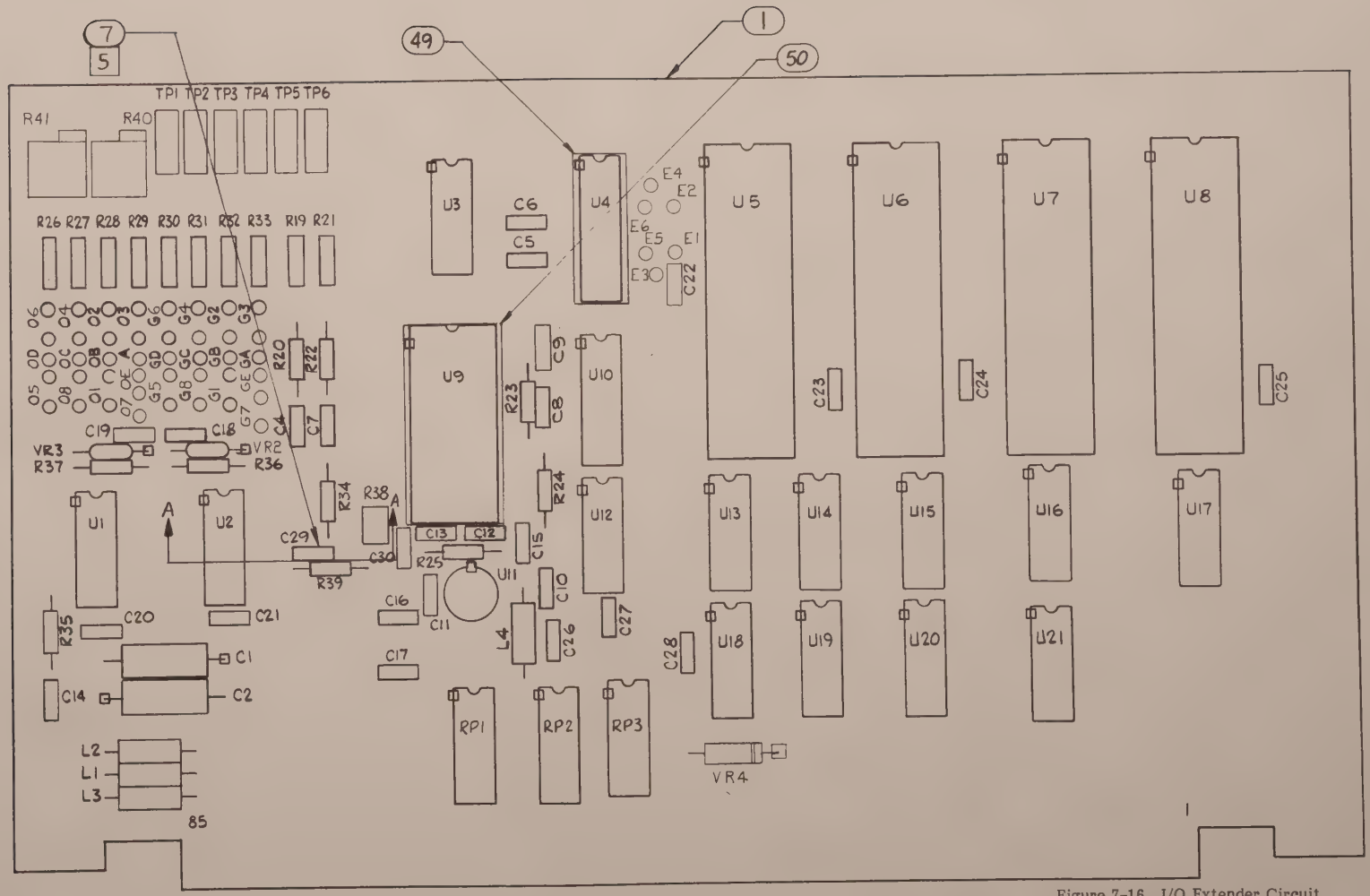


Figure 7-16. I/O Extender Circuit Card Assembly A6, Parts Location Diagram

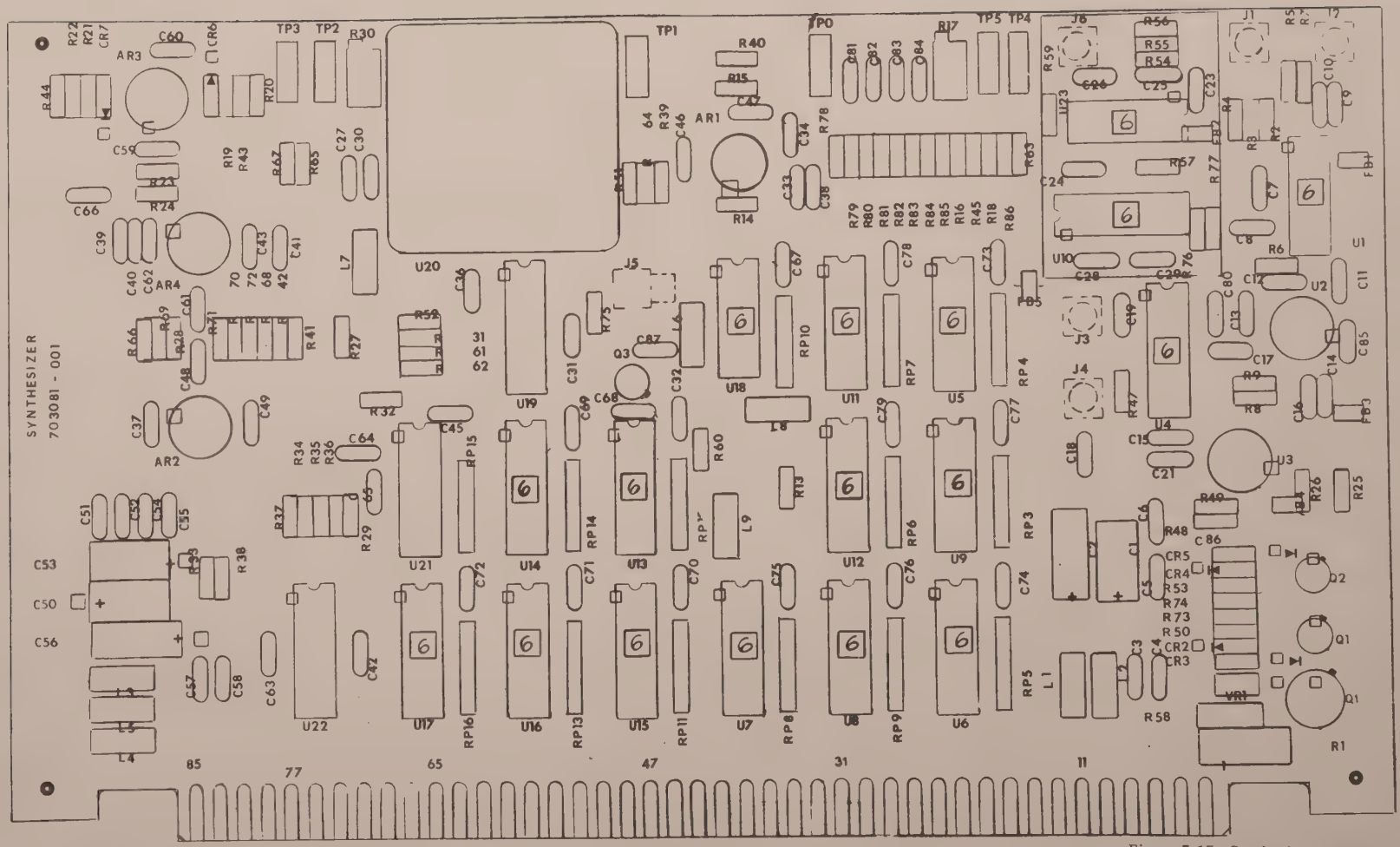


Figure 7-17. Synthesizer Circuit Card Assembly A7, Parts Location Diagram

703081C

INSTALLATION

CHAPTER 8

INSTALLATION

8-1. INTRODUCTION. This chapter contains detailed instructions, procedures, and requirements relative to installing the WJ-1204-1 Synthesized Signal Generator. Also included in this chapter is a checkout procedure to verify that the equipment operates correctly and within tolerance.

8-2. UNLOADING AND UNPACKING. The WJ-1204-1 is shipped in a sealed container bonded with special tape. Using appropriate equipment, transport the container to the installation site. Carefully place the container on a work bench and open it. Save container and packing materials for possible reshipment of equipment.

WARNING

Use care when lifting or moving the WJ-1204-1 to prevent damage to equipment or injury to personnel.

8-3. INSPECTION. Visually inspect the equipment for physical damage, and check that all items listed on the packing list are received. Examine the equipment for broken knobs, damaged connectors, and missing hardware. Examine RF and power cables for cuts and loose connectors. If there is any damage, immediately notify the proper authority.

8-4. REPACKING FOR RESHIPMENT. The following is a general rule for repacking for shipment. Pack instrument in original container. If original container is not available, proceed as follows:

a. If shipping to the manufacturer, attach a tag indicating the type of service required, return address, model number, and full serial number. If shipping to depot center for repair or storage, follow the procedures established for your ship, station, or company.

b. Wrap instrument in heavy paper or plastic before placing into an inner container.

c. Use plenty of shock-absorbing packing material around all sides of the instrument to prevent movement.

d. Place the WJ-1204-1 and inner container into a heavy carton or wooden box and seal with tape or metal bands.

e. Mark shipping crate with "DELICATE INSTRUMENT", "FRAGILE", etc.

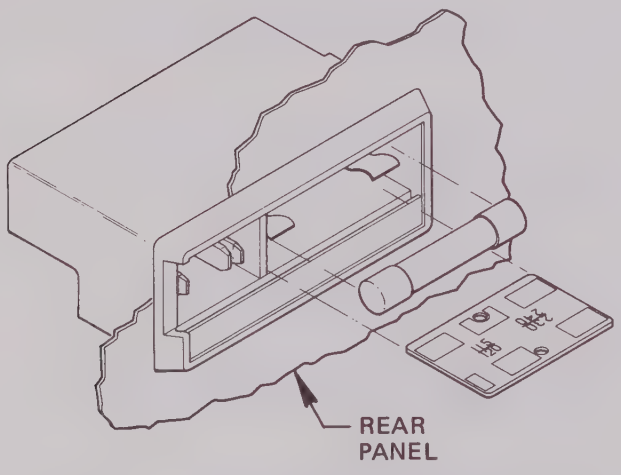
8-5. INPUT REQUIREMENTS.

WARNING

Before connecting the WJ-1204-1 to ac power, be sure that the 100-, 120-, 220-, 240-volt ac line selector (in the line filter assembly) is properly positioned as described in the following paragraph.

8-6. Line Voltage Requirements. This instrument is designed to operate on single phase 115/230 volts ac. Power required is approximately 250VA maximum. To avoid

instrument damage, the rear-panel line selector must be set to the correct position (100V, 120V, 220V, or 240V) and the correct fuse (see table 5-4) must be installed. The line selector is located in the ac line filter assembly just below the fuse. Remove the fuse from the filter assembly and check its rating. Next, firmly pull out the small circuit card with a needle-nose pliers. Reinsert the circuit card so that the 115/120 is facing you (for 115 V ac operation) or that the 230/240 is facing you (for 230 V ac operation) (see figure 8-1). When shipped from the factory, the switch is set for 120-volt ac operation.



78-L-021A

Figure 8-1. Ac Line Filter Assembly

8-7. Line Frequency Requirements. The WJ-1204-1 will operate at line frequencies between 47 and 420 Hz.

8-8. Ac Power Cable. To protect operating and servicing personnel, this instrument is equipped with a grounded three-conductor detachable 115/230 volt ac power cable. Connect the power cable to a 115 or 230 volt ac power source receptacle with a grounded third conductor. If the line power receptacle is a standard two-pin type instead of the three-pin type, use a two-to-three pin adapter and connect the pigtail to the receptacle ground screw.

8-9. Temperature Limits. Maximum allowable operating temperatures are 0 ^{o}C to +50 ^{o}C. If these limits are exceeded at the installation site, auxiliary cooling or heating should be used to keep the environment within limits. A space of at least three inches should be clear above, below, and behind the instrument to allow cooling air circulation.

8-10. BENCH OPERATION. The WJ-1204-1 is ready for bench operation as shipped from the factory.

8-11. RACK MOUNTING. To mount the instrument in a rack, it is necessary to order and install a rack flange kit from the manufacturer (Option AA).

CAUTION

Ambient temperature in rack during operation should not exceed +122 ^{o}F (50 ^{o}C). Be sure instrument position in rack permits adequate air circulation and that nearby equipment does not discharge hot air directly.

8-12. STORAGE. If the WJ-1204-1 is to be stored for an extended period of time, it should be enclosed in a clean, dry, sealed container. Storage environmental limitations are -40 ^{o}C to +75 ^{o}C.

CAUTION

During extended storage periods the WJ-1204-1 should be turned on for eight hours at six-month intervals. This procedure ensures that the life of the TWTA is prolonged. No RF signals through the TWTA are required for this procedure.

8-13. INSTALLATION CHECKOUT. The installation checkout procedures described in paragraphs 8-14, 8-15, and 8-16 ensure that the instrument is operating properly and within tolerances. References to other sections of this manual are made, where applicable, to avoid redundancy.

8-14. INSTALLATION INSPECTION AND PRE-ENERGIZING PROCEDURE. Table 8-1 is an installation inspection checklist that verifies that the equipment is ready for the initial turn-on as described in the following paragraph.

Table 8-1. Installation Inspection Checklist

Inspection Requirements	Date	Date	Date
1. Perform inspection described in paragraph 8-3.	1.	1.	1.
2. Verify that input requirements described in paragraph 8-5 are met.	2.	2.	2.
3. Verify that the test equipment listed in table 1-3 is available, is operating satisfactorily, and has been calibrated.	3.	3.	3.
4. Check that all field changes listed in table 1-4 have been accomplished.	4.	4.	4.
5. Ensure that the instrument is installed such that it is accessible for maintenance.	5.	5.	5.
6. Check that potential hazards do not exist and that it is otherwise safe to proceed with the initial turnon procedure.	6.	6.	6.

8-15. INITIAL TURN-ON PROCEDURE. The initial turn-on procedure consists of the normal turn-on procedure described in table 2-3. The only difference is as follows:

a. If the instrument has been inoperative (in storage, transit, etc.) less than one month, allow a 20 to 30-minute warm-up period.

b. If the instrument has been inoperative for over one month but less than six months, allow a four-hour burn-in period.

c. If the instrument has been inoperative for six months or more, allow an eight-hour burn-in period.

8-16. INSTALLATION VERIFICATION TEST. Do not begin this step until the procedures described in paragraphs 8-14 and 8-15 above have been satisfactorily completed. Record the results of this test in the Installation Standards Summary sheet. (It is recommended that the sheet be used as an original from which copies can be made; test results can then be recorded on the copies.) The Installation Verification Test verifies that frequency output, power output, and modulation capabilities are within specifications.

8-17. Frequency Accuracy. The purpose of this test is to confirm the frequency accuracy of 0.00035%. Proceed as follows:

a. Connect a calibrated frequency counter to the RF OUT port of the WJ-1204-1.

b. Configure the front panel controls as shown in table 8-2 (numbers in parentheses refer to figure 2-3):

c. Using front panel keyboard, program the frequencies shown in table 8-3 and verify that frequency is within limits:

NOTE

If discrepancy exists, attach an explanation to the Installation Standards Summary sheet, and refer to chapter 5 for troubleshooting procedures.

Table 8-2. Initial Control Settings

Control	Setting
Modulation Select (19)	OFF
MODE (3)	F
PROGRAM/DISPLAY (2)	F
ATTENUATION (dB) (6)	0
Power Meter Select (8)	INT

Table 8-3. Frequency Test Settings

Programmed frequency	Upper limit	Lower limit
0.1001 GHz	0.10010035	0.100099649
0.12499 GHz	0.124990437	0.124989562
0.12501 GHz	0.125010437	0.125009562
0.24999 GHz	0.249990875	0.249989125
0.25010 GHz	0.250100875	0.250099124
0.49990 GHz	0.499901749	0.499898250
0.50010 GHz	0.500101750	0.500098250
0.99990 GHz	0.999903500	0.999896500
1.0001 GHz	1.000103500	1.000096500
1.9999 GHz	1.999907000	1.999893000
2.0010 GHz	2.001007004	2.000992997
3.9990 GHz	3.999013997	3.998986004
4.0010 GHz	4.001014004	4.000985997
7.9990 GHz	7.999027997	7.998972004
8.0010 GHz	8.001028004	8.000971997
12.999 GHz	12.9990455	12.9989545
13.001 GHz	13.0010455	13.0009545
17.999 GHz	17.999063	17.998937
18.001 GHz	18.001063	18.000937
22.000 GHz	22.000077	21.999923

8-18. RF Power Output. The purpose of this test is to confirm ±1 dB accuracy of the internal power meter: a minimum leveled output power of 0 dBm, a minimum unleveled output power of +5 dBm, and proper operation of the internal 0-90 dB attenuator. Proceed as follows:

a. Connect a calibrated power meter to the RF OUT connector of the WJ-1204. For frequencies above 18 GHz, connect a power head directly to the RF OUT port (Hewlett-Packard Model K486A recommended).

b. Configure front panel controls as shown in table 8-2.

c. Press the CAL button momentarily.

d. Using keyboard, select the frequencies shown in table 8-4. For each frequency programmed, adjust the LEVEL control so that external power meter indicates 0 dBm. Verify that the RF POWER (dBm) display is within ±1 dB of external measurement.

NOTE

If discrepancy exists, attach an explanation to the Installation Standards Summary sheet, and refer to chapter 5 for troubleshooting procedures.

e. Program 1 GHz and, using the LEVEL control, vary the output power as shown in table 8-5. Verify that the displayed RF output is within ±1 dB of externally measured power.

f. Remove the power meter from the WJ-1204-1, and connect a spectrum analyzer to the RF OUT port.

g. Using the same frequency as in step (e) above, adjust the LEVEL control for a 0 dBm reference level as indicated on the spectrum analyzer.

h. Vary the ATTENUATION (dB) control from 0 to 90, and verify that the output signal level is reduced approximately 10 dB at each setting.

Table 8-4. Output Power Test Data

Programmed frequency	Externally measured power output
0.11250 GHz	0 dBm
0.18750 GHz	0 dBm
0.37500 GHz	0 dBm
0.75000 GHz	0 dBm
1.5000 GHz	0 dBm
3.0000 GHz	0 dBm
6.0000 GHz	0 dBm
10.500 GHz	0 dBm
15.500 GHz	0 dBm
22.000 GHz	0 dBm

Table 8-5. RF Power Display Test

Externally measured power output	Acceptable displayed RF power limits
+5 dBm	+4 to +6 dBm
+4 dBm	+3 to +5 dBm
+3 dBm	+2 to +4 dBm
+2 dBm	+1 to +3 dBm
+1 dBm	0 to +2 dBm
0 dBm	-1 to +1 dBm
-1 dBm	-2 to 0 dBm
-2 dBm	-3 to -1 dBm
-3 dBm	-4 to -2 dBm
-4 dBm	-5 to -3 dBm
-5 dBm	-6 to -4 dBm
-6 dBm	-7 to -5 dBm
-7 dBm	-8 to -6 dBm
-8 dBm	-9 to -7 dBm
-9 dBm	-10 to -8 dBm

NOTE

If any discrepancy exists, attach an explanation to the Installation Standards Summary sheet, and refer to chapter 5 for trouble-shooting procedures.

8-19. Frequency Sweep Mode. The purpose of this test is to verify that the WJ-1204-1 sweeps between the programmed limits. Proceed as follows:

a. Connect a calibrated frequency counter to the RF OUT port of the WJ-1204-1.

b. Configure front panel controls as shown in table 8-2 except set INCREMENT switch to 1 MHz position.

c. Program any frequency within the range of the WJ-1204-1 and adjust the power output to 0 dBm output.

d. Using the PROGRAM/DISPLAY pushbuttons, sequentially program the start and stop frequencies shown in table 8-6. (Detailed instructions for entering the sweep mode is provided in table 2-4.) Verify that the output sweeps across the entire programmed limits in 1 MHz steps.

NOTE

Note any discrepancies no a separate sheet and attach to Installation Standards Summary sheet; refer to chapter 5 for troubleshooting procedures.

8-20. ΔF Mode. The purpose of this test is to verify that the WJ-1204-1 varies about a center frequency. Proceed as follows:

a. Connect a spectrum analyzer to the RF OUT port of WJ-1204-1.

b. Configure front panel controls as shown in table 8-2.

c. Program any frequency within the range of the WJ-1204-1.

d. Set the MODE control to the F $\pm$ ΔF position. Verify that the output frequency, as displayed on spectrum analyzer, varies in the negative and positive direction from the programmed frequency.

Table 8-6. Frequency Sweep Limits

Start frequency	Stop frequency
0.10000 GHz	0.12500 GHz
0.12500 GHz	0.25000 GHz
0.25000 GHz	0.50000 GHz
0.50000 GHz	1.0000 GHz
1.0000 GHz	2.0000 GHz
2.0000 GHz	4.0000 GHz
4.0000 GHz	8.0000 GHz
8.0000 GHz	13.000 GHz
13.000 GHz	18.000 GHz
18.000 GHz	26.000 GHz

8-21. Square Wave Modulation. The purpose of this test is to verify that the output frequency is modulated by a 1 kHz square wave. Proceed as follows:

a. Connect an oscilloscope to the RF OUT port through a detector.

b. Connect the SYNC OUT port of the WJ-1204-1 to the trigger input of oscilloscope.

c. Configure front panel controls as shown in table 8-2.

d. Program any frequency within the range of the WJ-1204-1.

e. Press the SQUARE WAVE switch on the Modulation Select control.

f. Observe oscilloscope and verify that a 1 kHz square wave is present.

NOTE

Note any discrepancy on a sheet and attach to Installation Standards Summary sheet; refer to chapter 5 for troubleshooting procedures.

8-22. Pulse Modulation. The purpose of this test is to verify that the instrument pulse-modulates the RF output. Proceed as follows:

a. Repeat steps (a) through (d) of paragraph 8-21 above.

b. Press the PULSE switch on the Modulation Select control.

c. Set thumbwheel switches to 00.1 μs and verify that oscilloscope measures the selected pulse width.

d. Repeat step c for 1 μs and for 10 μs.

NOTE

Note any discrepancies on a separate sheet and attach to Installation Standards Summary sheet; refer to chapter 5 for troubleshooting procedures.

SYNTHESIZED SIGNAL GENERATOR WJ-1204-1

INSTALLATION STANDARDS SUMMARY

Date_____

Serial Number_____

Installed in

_____

Name of person performing installation

_____

Record on this summary sheet the test indications which have been obtained during the installation verification test, paragraph 8-16.

Paragraph Number	Procedural Step		
8-17	a.	_____	Check
	b.	_____	Check
	c.	Programmed Frequency (GHz)	Output Frequency (GHz)
		0.1001 GHz	_____
		0.12499 GHz	_____
		0.12501 GHz	_____
		0.24999 GHz	_____
		0.25010 GHz	_____
		0.49990 GHz	_____
		0.50010 GHz	_____
		0.99990 GHz	_____
		1.0001 GHz	_____
		1.9999 GHz	_____
		2.0010 GHz	_____
		3.9990 GHz	_____
		4.0010 GHz	_____
		7.9990 GHz	_____
		8.0010 GHz	_____
		12.999 GHz	_____
		13.001 GHz	_____

Paragraph Number	Procedural Step		
8-17 (Con't)	c.	Programmed Frequency (GHz)	Output Frequency (GHz)
		17.999 GHz	_____
		18.001 GHz	_____
		22.000 GHz	_____
8-18	a.	_____	Check
	b.	_____	Check
	c.	_____	Check
	d.	Programmed Frequency	Internally Indicated Power Out
		0.11250 GHz	_____ dBm
		0.18750 GHz	_____ dBm
		0.37500 GHz	_____ dBm
		0.75000 GHz	_____ dBm
		1.5000 GHz	_____ dBm
		3.0000 GHz	_____ dBm
		6.0000 GHz	_____ dBm
		10.500 GHz	_____ dBm
		15.500 GHz	_____ dBm
		22.000 GHz	_____ dBm
	e.	Frequency _____ GHz	
		Externally Measured Power Output	Internally Indicated Power Output
		+5 dBm	_____ dBm
		+4 dBm	_____ dBm
		+3 dBm	_____ dBm
		+2 dBm	_____ dBm
		+1 dBm	_____ dBm
		0 dBm	_____ dBm
		-1 dBm	_____ dBm
		-2 dBm	_____ dBm
		-3 dBm	_____ dBm
		-4 dBm	_____ dBm
		-5 dBm	_____ dBm
		-6 dBm	_____ dBm
		-7 dBm	_____ dBm
		-8 dBm	_____ dBm
		-9 dBm	_____ dBm

Paragraph Number	Procedural Step			
8-18 (Con't)	f.	_____		Check
	g.	_____		Check
	h.	Attenuation Setting	Analyzer Measurement	
		0 dBm	_____ dBm	
		10 dBm	_____ dBm	
		20 dBm	_____ dBm	
		30 dBm	_____ dBm	
		40 dBm	_____ dBm	
		50 dBm	_____ dBm	
		60 dBm	_____ dBm	
		70 dBm	_____ dBm	
		80 dBm	_____ dBm	
		90 dBm	_____ dBm	
8-19	a.	_____		Check
	b.	_____		Check
	c.	_____		GHz
	d.	Start Frequency	Stop Frequency	
		.10000 GHz	0.12500 GHz _____	Check
		0.12500 GHz	0.25000 GHz _____	Check
		0.25000 GHz	0.50000 GHz _____	Check
		0.50000 GHz	1.0000 GHz _____	Check
		1.0000 GHz	2.0000 GHz _____	Check
		2.0000 GHz	4.0000 GHz _____	Check
		4.0000 GHz	8.0000 GHz _____	Check
		8.0000 GHz	13.000 GHz _____	Check
		13.000 GHz	18.000 GHz _____	Check
		18.000 GHz	26.000 GHz _____	Check
8-20	a.	_____		Check
	b.	_____		Check
	c.	_____		GHz
	d.	_____		Check

INSTALLATION STANDARDS SUMMARY -Continued

Paragraph Number	Procedural Step		
8-21	a.	_____	Check
	b.	_____	Check
	c.	_____	Check
	d.	_____	GHz
	e.	_____	Check
	f.	_____	Check
8-22	a.	_____	Check
	b.	_____	Check
	c.	_____	μs
	d.	_____	μs
		_____	μs

APPENDIX A

Users Note for WJ-1204-1 Option AB

General Purpose Interface Bus, (GPIB) IEEE STD-488-1978

USERS NOTE: WJ-1204 SERIES STANDARD BUS INTERFACE

1.0 INTRODUCTION

This Users Note is designed to aid the software and hardware development necessary to use the WJ-1204 Series Standard Interface.

2.0 GENERAL DESCRIPTION

The WJ-1204 Series Standard Bus Interface is based on the precept that the WJ-1204 series unit is an addressable listener and talker, and the Controller, a computer, minicomputer, or calculator, is capable of controlling an HP-IB or IEEE 488-1978 compatible interface. The interface uses an eight bit Bus and three handshake lines; DAV, controlled by the talker, and NRFD and NDAC, controlled by the listener. Along with these lines is an attention (ATN) control line controlled by the controller which is used to define the state of the Data Bus. Several additional lines are available for use by the controller. Their meaning and use is discussed in IEEE Standard Digital Interface for Programmable Instrumentation. Number 488-1978.

Table 1 is an outline of the Interface I/O lines and their uses. Figure 1 is a Standard Bus Interface Connector.

2.1 Capabilities

This section describes the basic capabilities of the WJ-1204 Series Unit equipped with the Standard Bus Interface. All references are to the IEEE Standard Digital Interface for Programmable Instrumentation IEEE STD-488-1978.

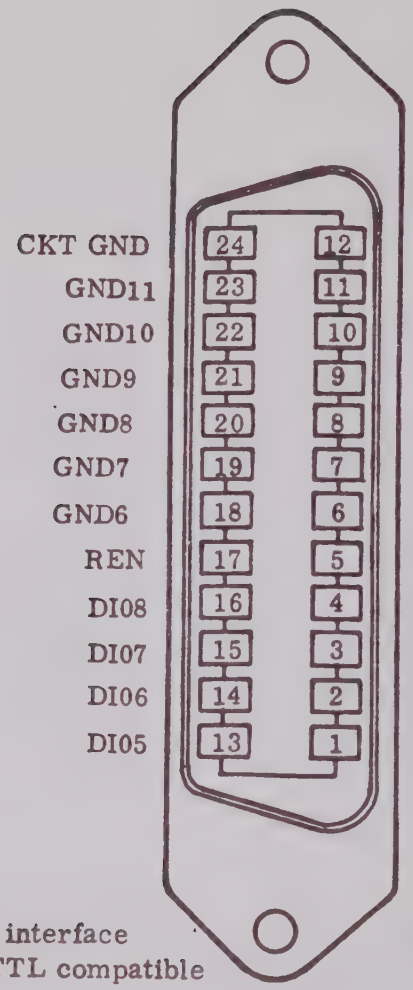
2.1.1 Interface Subset Capability

The Standard Bus Interface has the following subset capability as outlined in Appendix C of the IEEE 488-1978 standard and specified throughout the standard SH1, AH1, T6, TEO, L4, LEO, SRI, RLO, PPO, DCO, DT1 and CO.

STANDARD BUS INTERFACE INPUT/OUTPUT LINES

NAME	MEANING	CONTROLLING SOURCE	IDENTIFICATION/USE	COMMENTS
DI01 ↓ DI07	Data Input-Output One ↓ Data Input-Output Seven	Talker or controller ↓ Talker or controller	LSB of ASCII character ↓ MSB of ASCII character	These lines are used for the general exchange of information in both command and data modes.
DI08	Data Input-Output Eight	Talker or controller	Parity check bit*	
DAV NRFD NDAC	Data Valid Not Ready for Data Not Data Accepted	Talker or controller Listener Listener	Data on DI01-8 is valid Listener is busy Listener has not yet accepted the data	These lines are used for asynchronous data transfer using the handshake sequence.
IFC	Interface Clear	Controller .	Unaddresses all talkers and listeners	Management control lines to govern the state and use of the interface bus.
ATN	Attention	Controller	When high-data mode When low--command mode	
SRQ	Service Request	Any unit on the interface bus	Set low when a unit requires servicing	
REN	Remote Enable	Controller	Must be low for the information on the interface bus to be valid.	
EOI	End or Identify	Talker or controller	Indicates the end of a multi-byte data transfer, also used in parallel polling**	

LSB	Least Significant Bit
MSB	Most Significant Bit
ASCII	American Standard Code for Information Interchange
Listener	A device capable of receiving data or commands from other instruments
Talker	A device capable of transmitting data to other instruments
Controller	A device capable of managing communications over the interface bus
*	The parity check bit is not recognized by the present interface board
**	The EOI line is not recognized or activated ' the present interface board



The standard bus interface logic levels are TTL compatible (negative true)

MATING CONNECTOR
Amphenol 57-30240(383)

Figure 1 - Standard Bus Interface Connector Pin-Outs.

aa33679

2.1.2 Talk/Listen Addresses

Both the talk and listen addresses for the WJ-1204 Series Units are manually programmable via a mini-dip switch located on the bottom of the mother board assembly. The WJ-1204 Synthesizer Mainframe is shipped with the talk address set at "S"* and the listen address set at "3" *.

2.2 Unit Talk Characteristics

The WJ-1204 Synthesizer Mainframe has two talk modes which are important to central-operator-run test systems and to automatically controlled test systems. These are the Power Meter reading and Service Request for invalid frequencies.

2.2.1 Normal Talk

The Standard Bus Interface conveys the Power Meter reading, when told by the controller to talk, in 4 bytes of data.

1st byte	SIGN
2nd byte	10 dbm digit
3rd byte	1 dbm digit
4th byte	.1 dBm digit

The transmission is terminated with the EOI signal

2.2.2 Serial Poll Talk

The Standard Bus Interface has the ability to respond to a serial poll by the system controller. This is done by the controller enabling a serial poll with the ASCII Character "CAN", in the Bus Command Mode, and addressing successive instruments on the Bus to talk. When addressed, the synthesizer will, if it has requested service by setting the SRQ line low, set DIO line 7 low. If it had not set SRQ low DIO line 7 will be high. After a serial poll is complete, the synthesizer must be commanded to disable the serial poll with the ASCII character "EM", in the Bus command mode.
in Section 2.2.1.

* ASCII Character

2.3 Unit Listen Characteristics

The WJ-1204 has one listen mode which is used for remote control of the synthesizer frequency. The frequency programming command consists of a frequency specified in GHz followed by the ASCII character "E". The EOI signal is not required.

Examples:

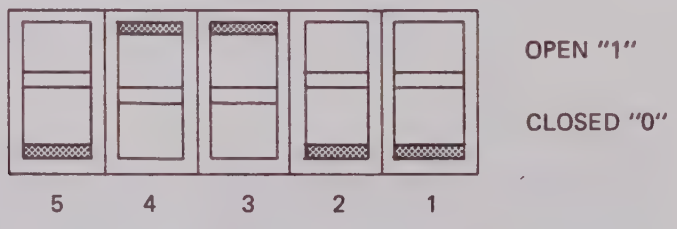
"21.34E"	21.34 GHz
"15E"	15 GHz
"0.12E"	.12 GHz
"5E"	5 GHz

3.0 Operation

The following paragraphs discuss the basic methods needed to control the WJ-1204 using the IEEE Standard Interface Bus.

3.1 Address Selection

The address select dip switch located on bottom of mother board must be set to desired IEEE device address. Open for binary 1, closed for binary 0.



The IEEE listen address "3" and talk address "S" are shown above.

3.2 Front Panel Controls

The modulation select and power meter select switches are not software controlled and should be selected before operating. The modulation select will normally be in the OFF position and the power meter will be INT. All other controls will be disabled during remote operation.

3.3 Local - Remote Selector

The LOC/REM selector switch located on rear panel near IEEE Bus connector must be placed in the REM (Remote) position for remote operation.

3.4 Initialization

The WJ-1204 can be initialized either through the power on sequence or by issuing an "IFC" command. The synthesizer is then ready to be programmed using an IEEE controller.

MP MASTER
MA34475